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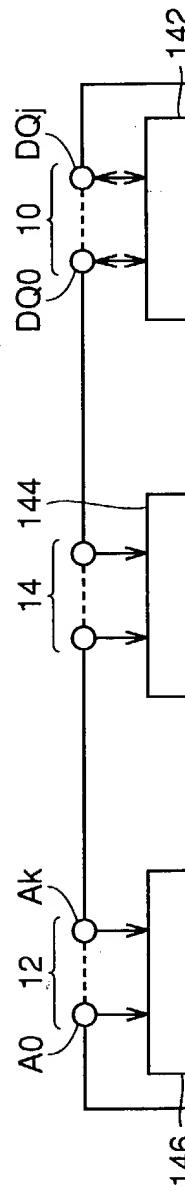
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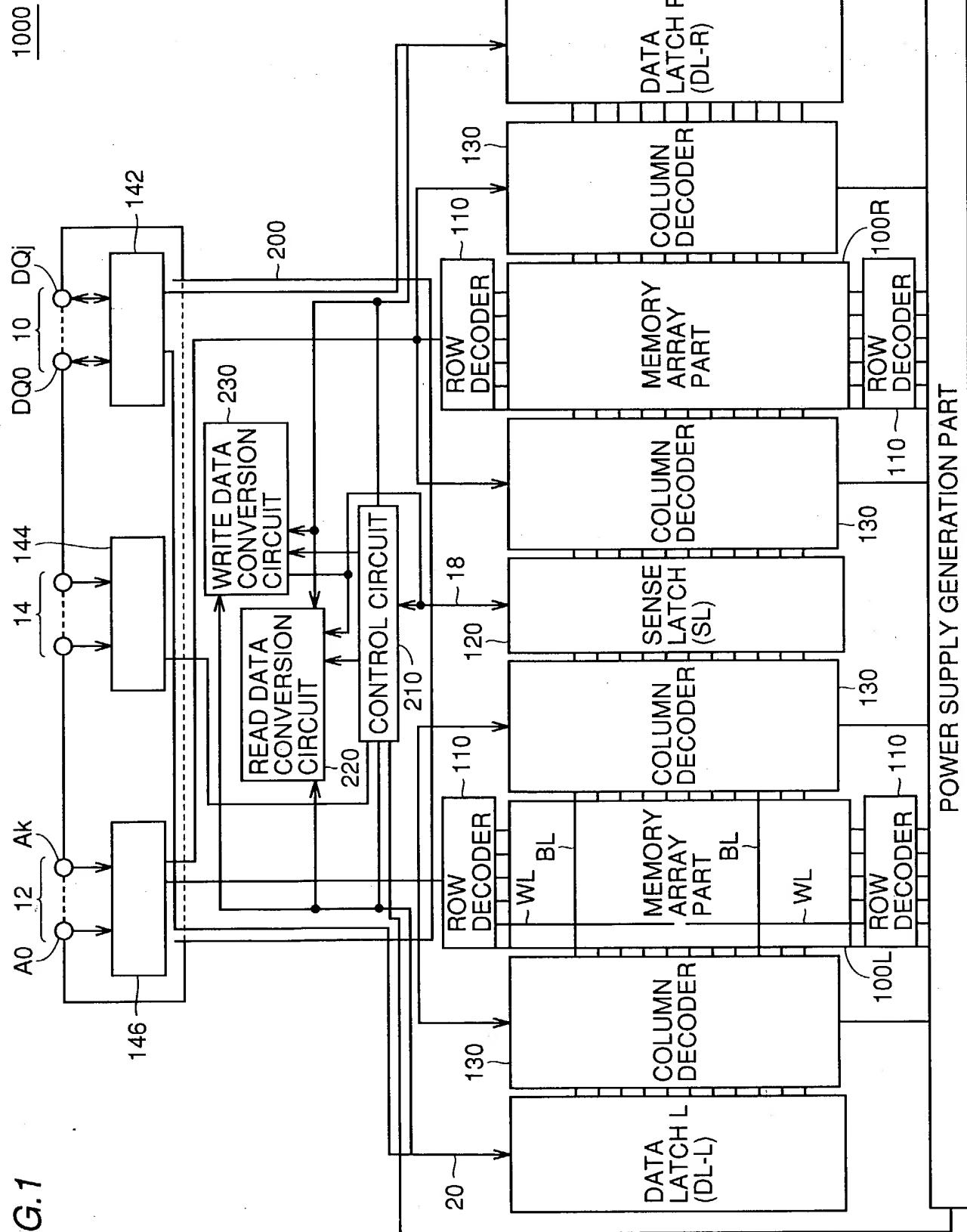
F/G. 1

1000



146

142



150

POWER SUPPLY GENERATION PART



FIG.2

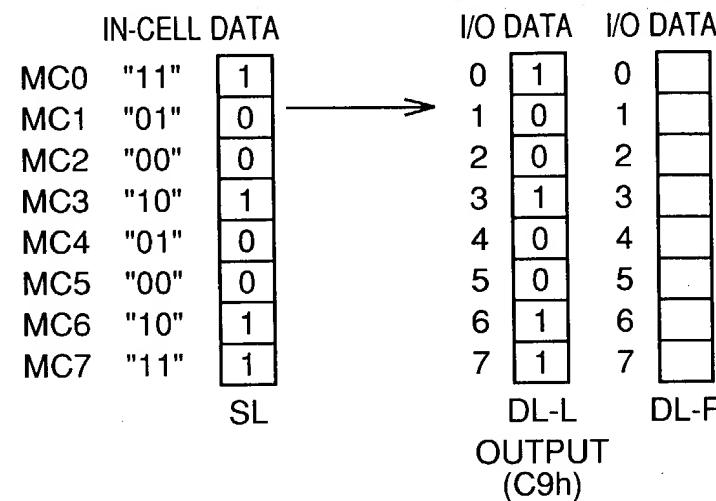


FIG.3

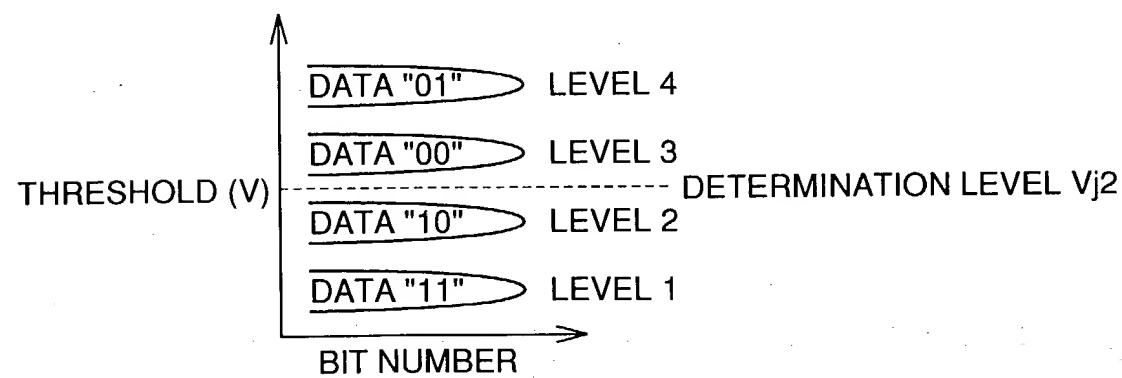




FIG.4

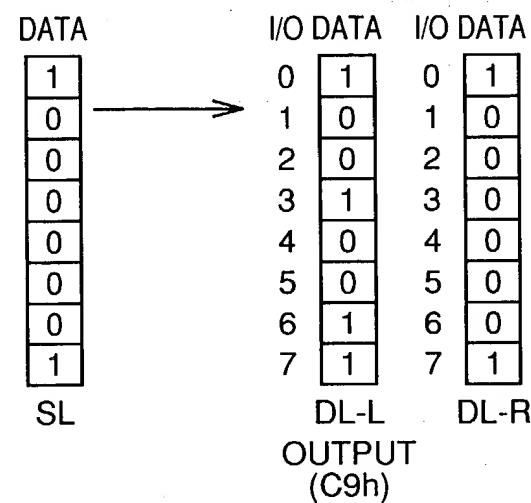


FIG.5

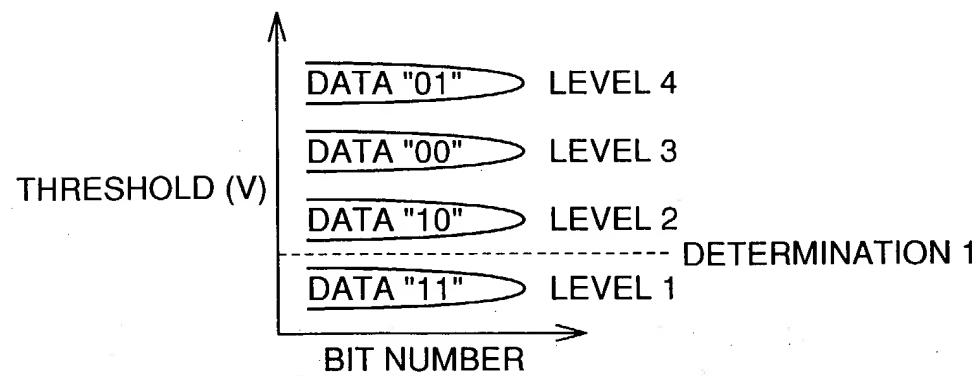




FIG.6

DATA	OPERATION	I/O DATA	I/O DATA
1		0	1
0		1	1
1		2	0
1		3	1
0		4	0
1		5	0
1		6	1
1		7	1
SL		DL-L	DL-R
		OUTPUT	
		(C9h)	

FIG.7

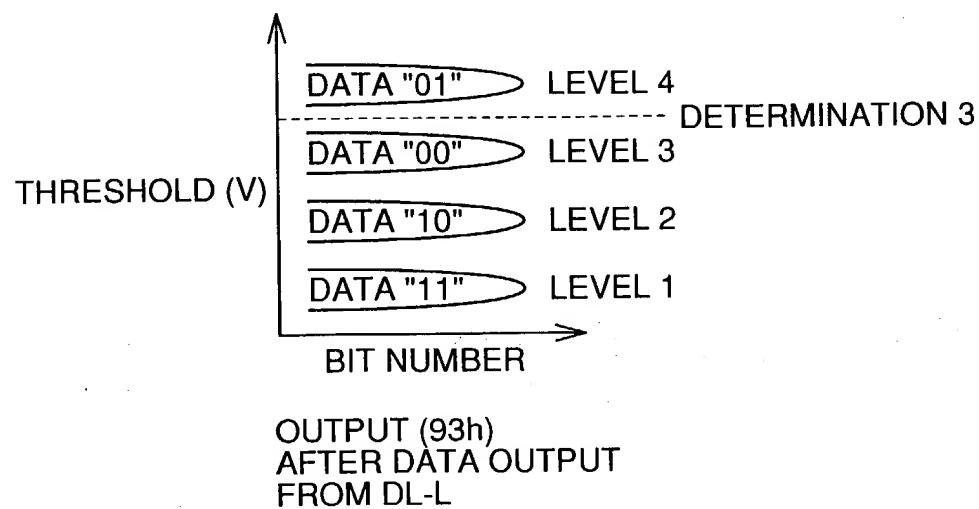




FIG. 8

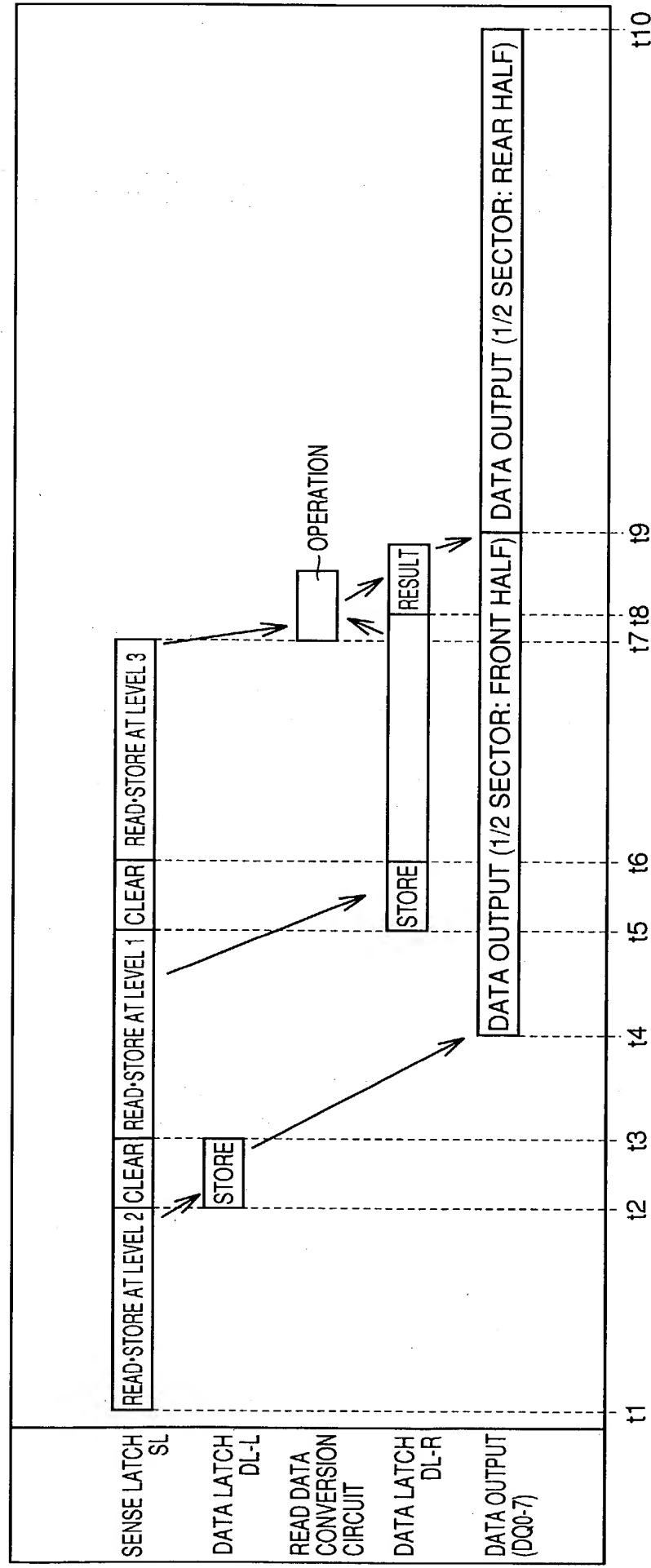




FIG.9

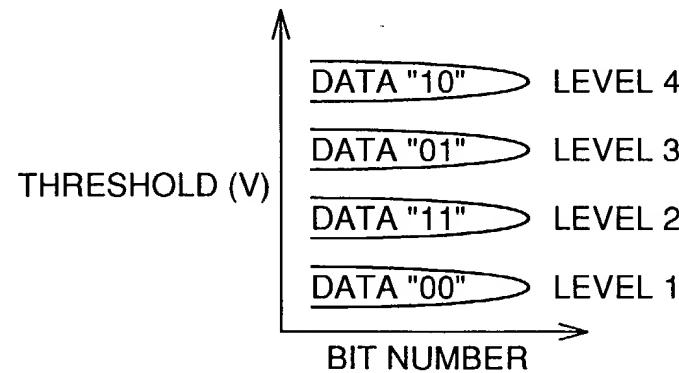


FIG.10

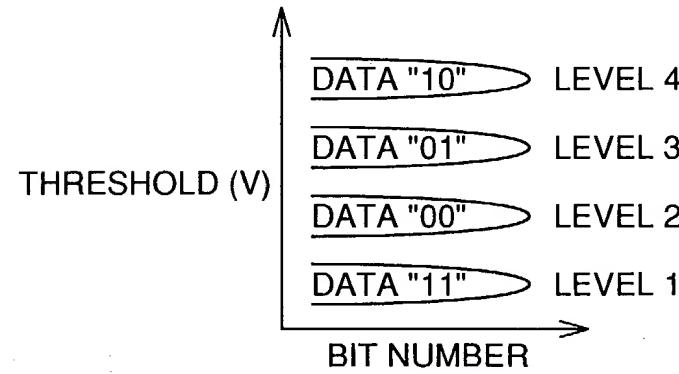




FIG. 11

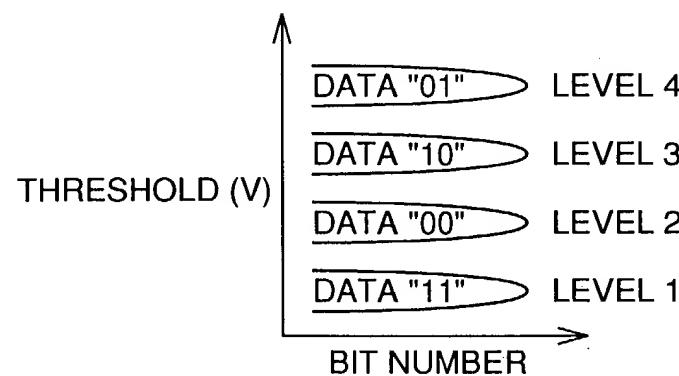


FIG. 12

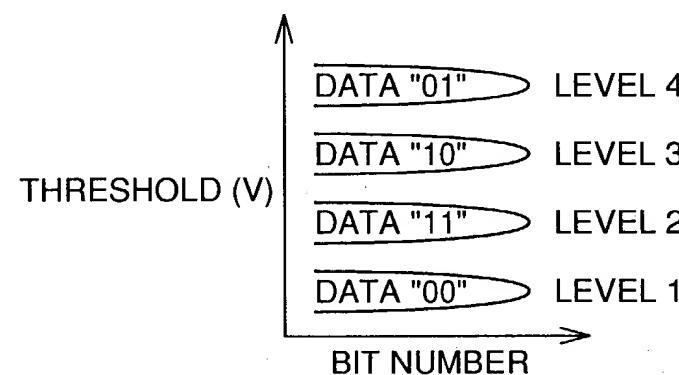




FIG. 13

IN-CELL DATA		I/O DATA	I/O DATA
"11"	1	0	0
"00"	0	1	1
"01"	0	2	2
"10"	0	3	3
"00"	0	4	4
"01"	0	5	5
"10"	0	6	6
"11"	1	7	7
	SL	DL-L	DL-R
		OUTPUT	
		(C9h)	

"0" ONLY
WHEN "0"
IN SL AND
"1" IN DL-R

FIG. 14

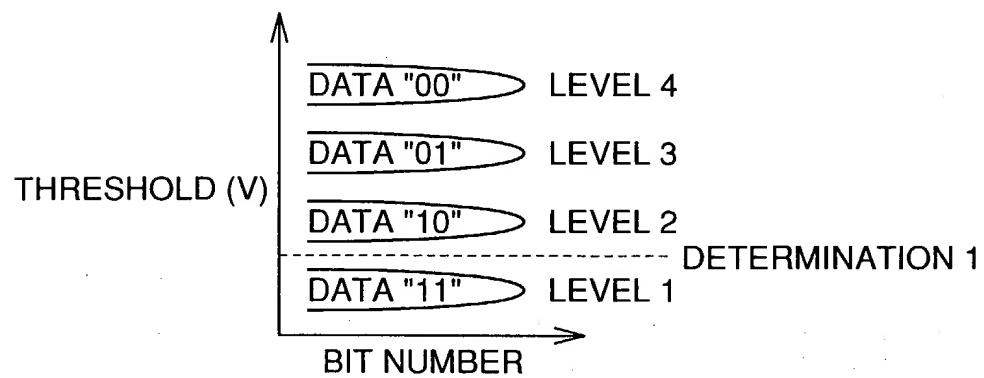




FIG. 15

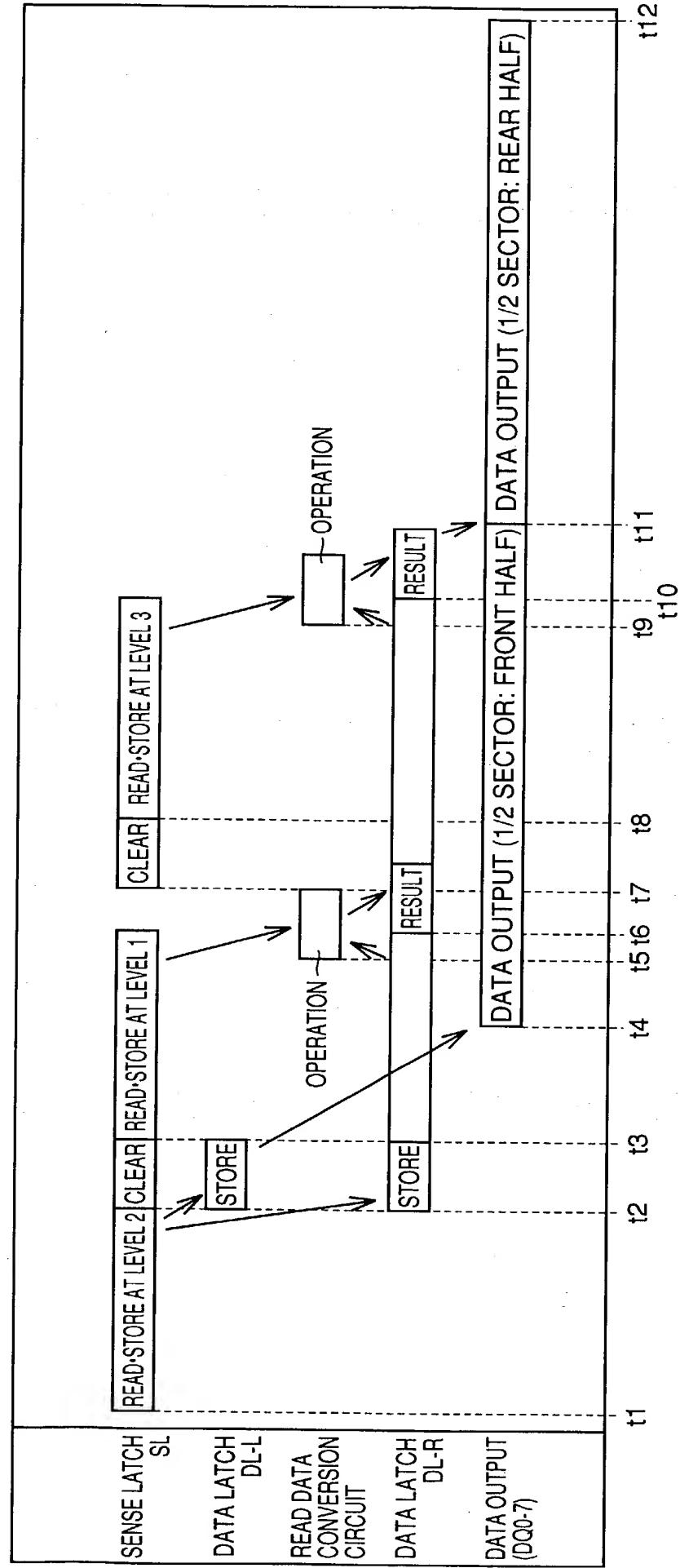


FIG. 16A

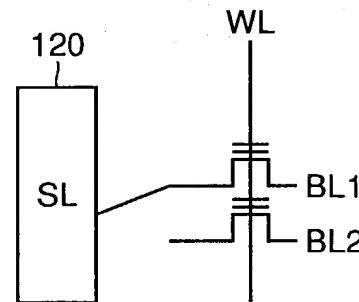


FIG. 16B

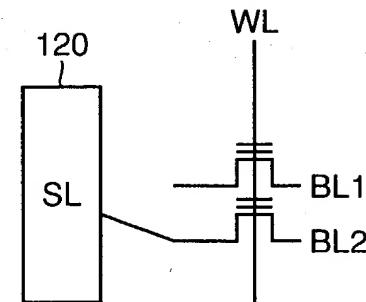


FIG. 17

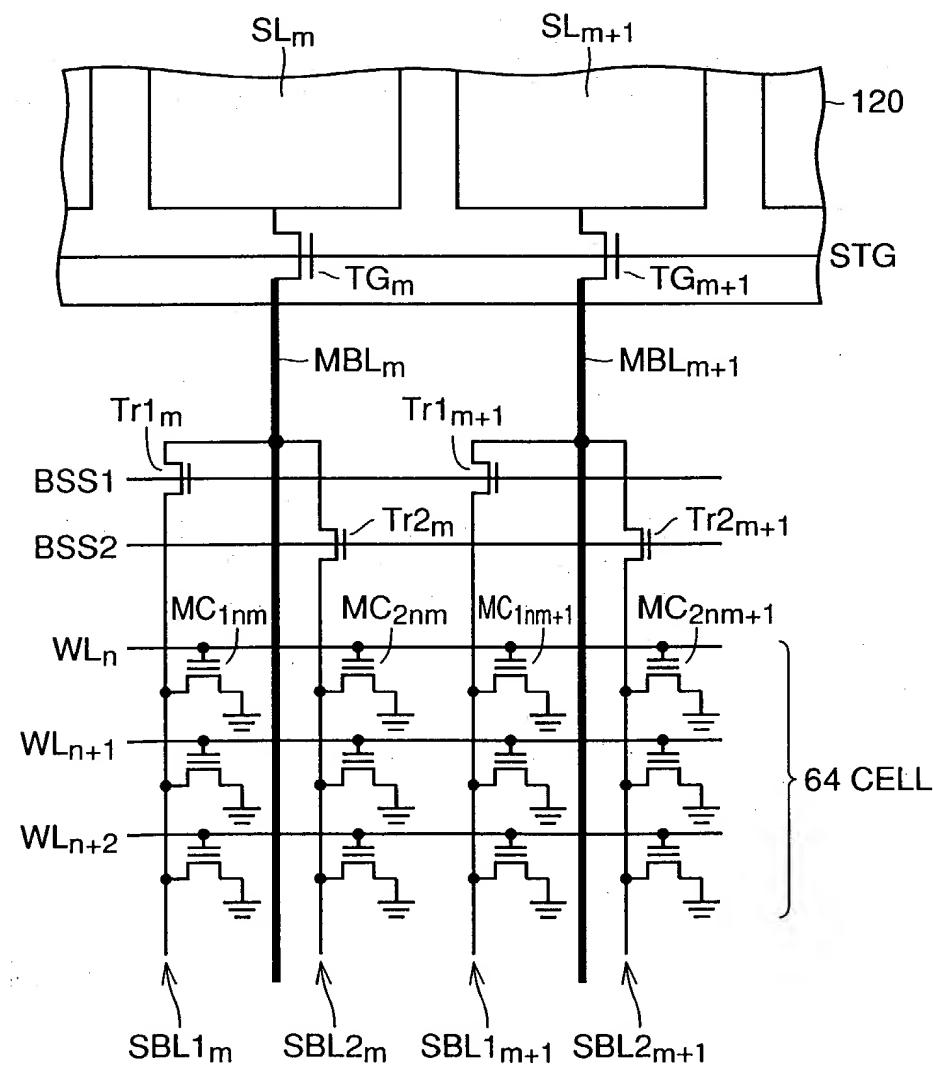




FIG. 18

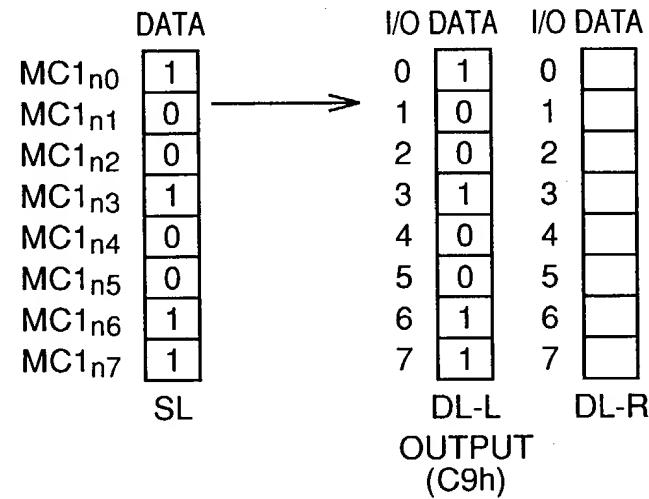


FIG. 19

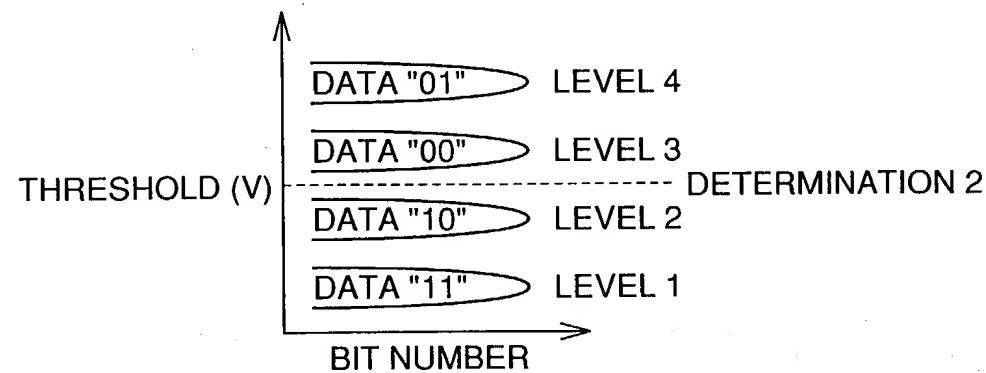




FIG.20

DATA	I/O DATA	I/O DATA
1	0	0
0	1	1
0	0	0
1	3	3
0	4	4
0	5	5
1	6	6
1	7	7

SL DL-L DL-R

OUTPUT
(C9h)

FIG.21

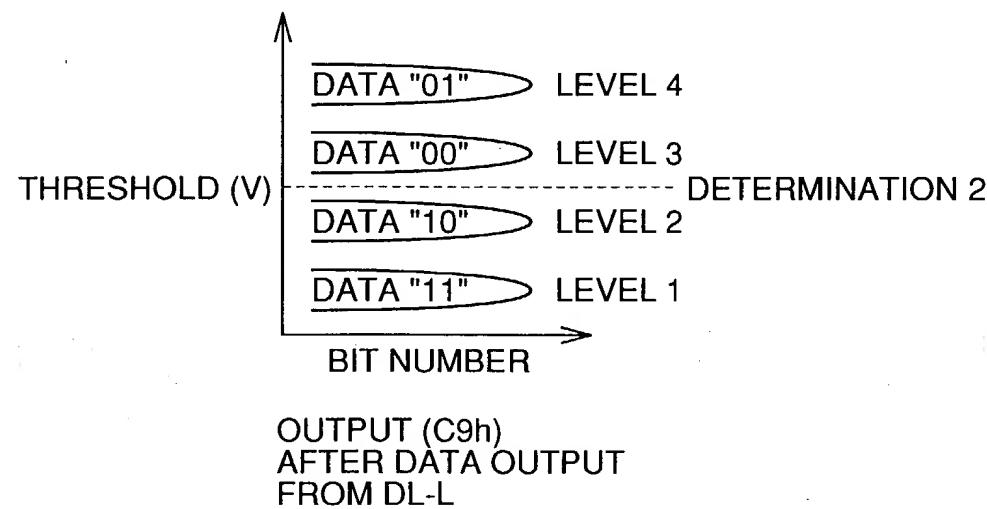




FIG.22

DATA

1
0
0
0
0
0
0
1

SL

→

I/O DATA

0	1
1	0
2	0
3	0
4	0
5	0
6	0
7	1

DL-L

I/O DATA

0	1
1	0
2	0
3	1
4	0
5	0
6	1
7	1

DL-R

OUTPUT
(C9h)

FIG.23

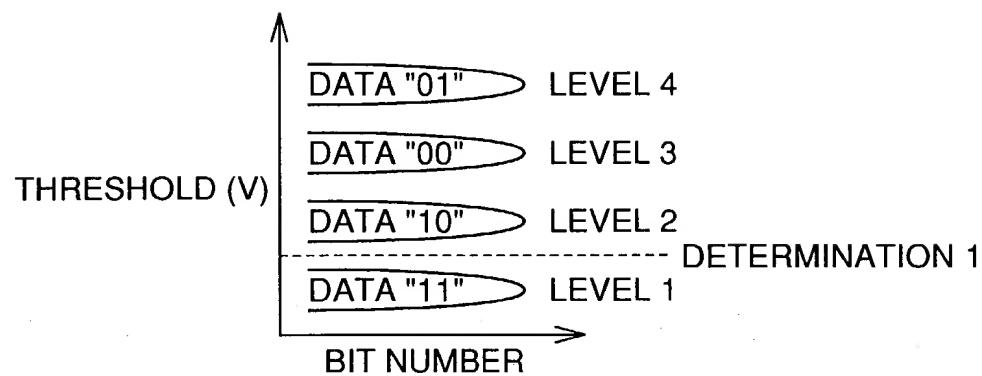




FIG.24

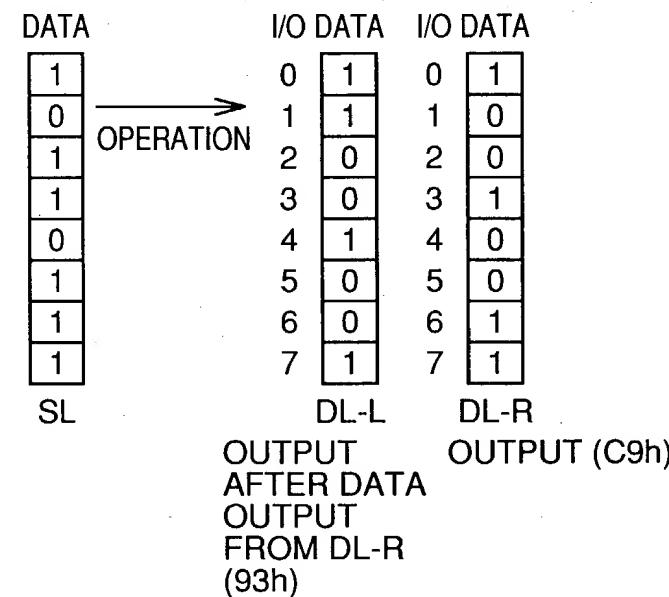


FIG.25

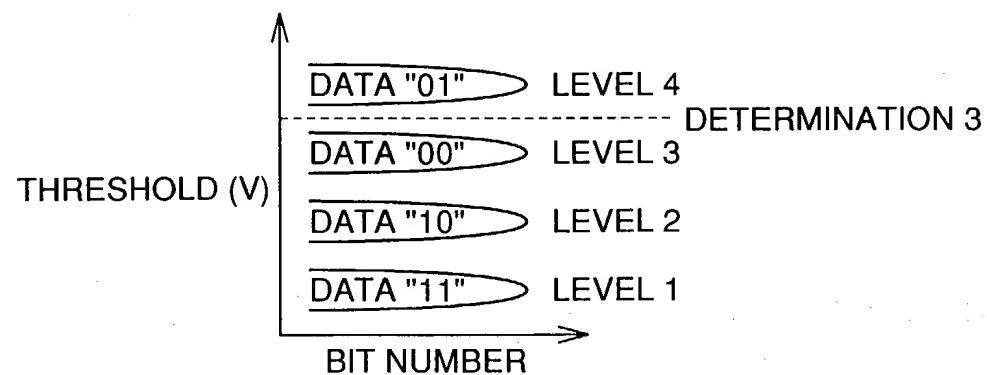




FIG.26

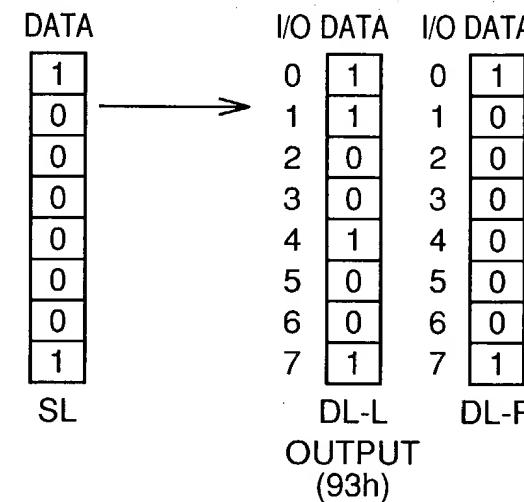


FIG.27

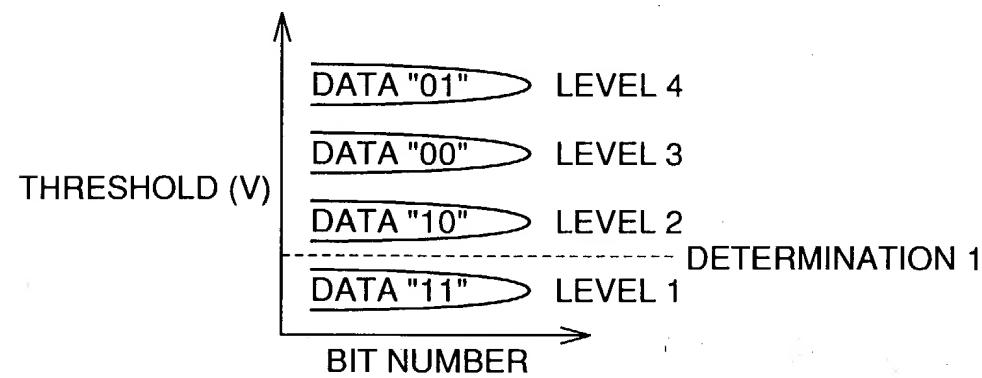




FIG.28

DATA	I/O DATA	I/O DATA
1	0	0
0	1	1
1	1	1
1	2	2
0	0	0
1	3	3
0	4	4
1	1	1
1	5	5
1	0	0
0	6	6
1	0	0
1	7	7
SL	DL-L	DL-R
	OUTPUT (93h)	OUTPUT (93h)
		AFTER DATA OUTPUT FROM DL-L

FIG.29

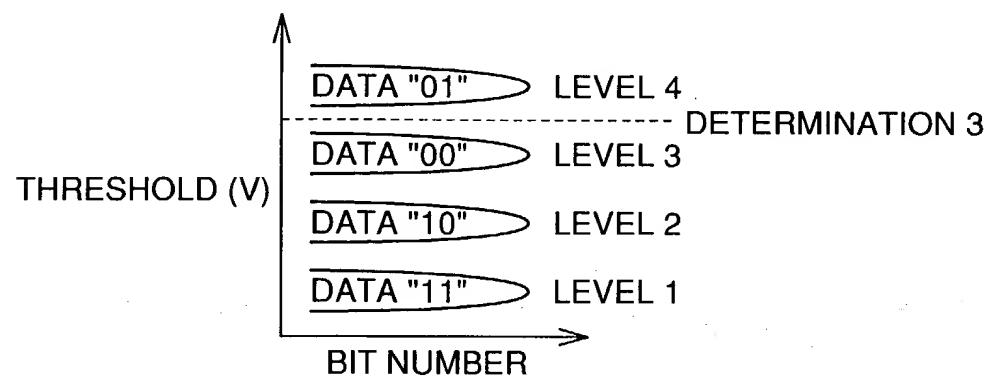




FIG. 30

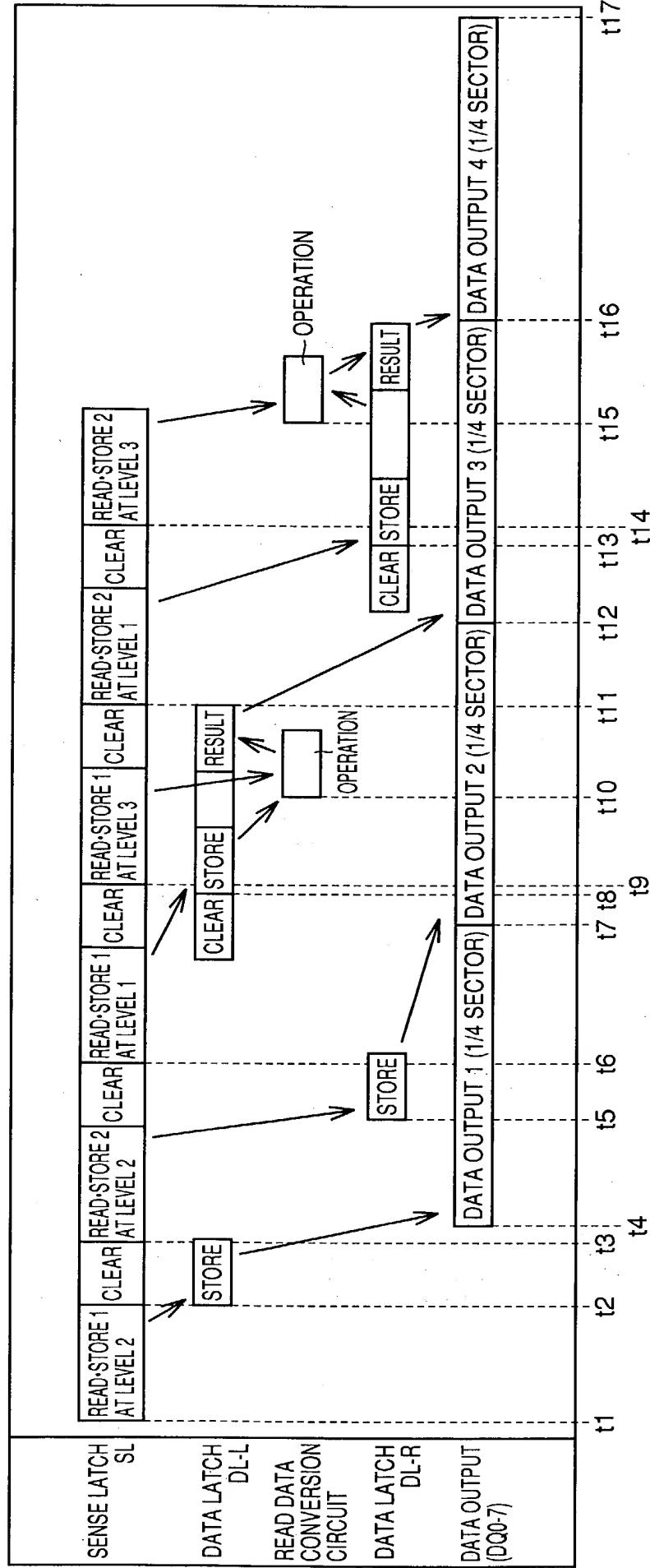




FIG.31

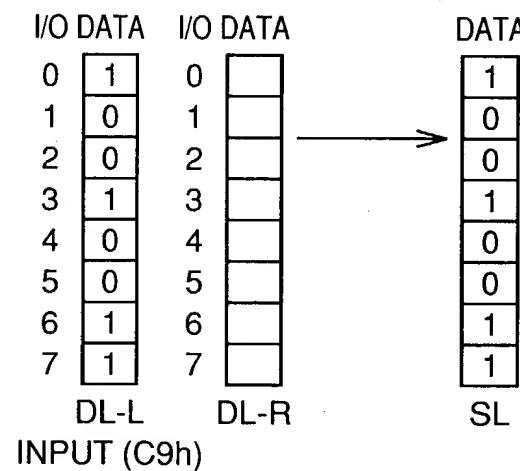


FIG.32

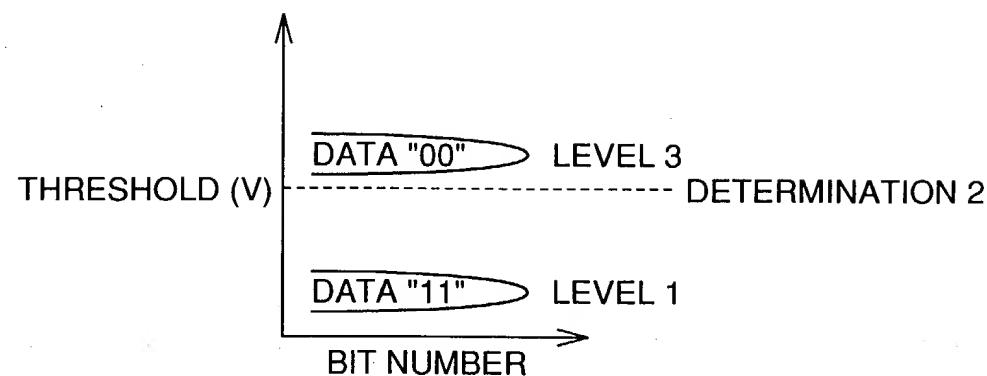




FIG.33

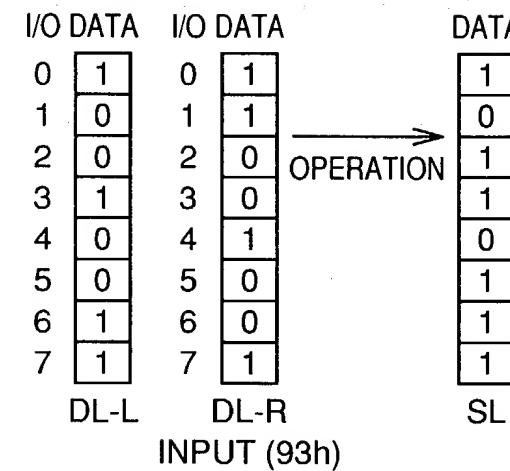


FIG.34

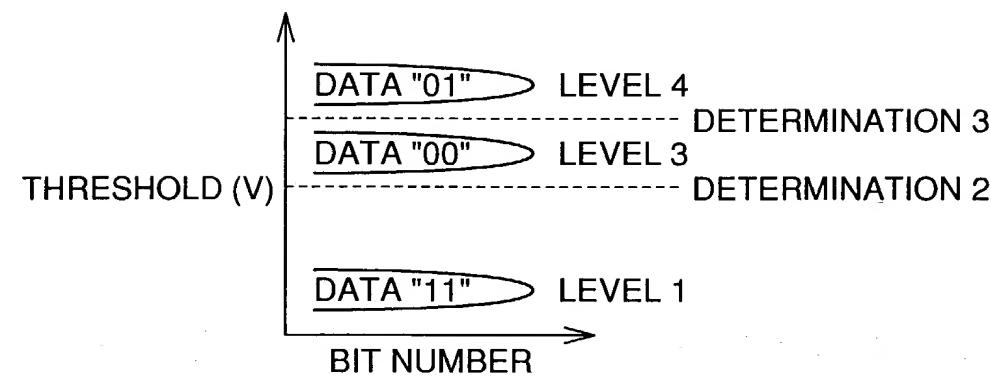




FIG.35

I/O DATA	I/O DATA	DATA
0 1	0 1	1
1 0	1 1	1
2 0	2 0	1
3 1	3 0	0
4 0	4 1	1
5 0	5 0	1
6 1	6 0	0
7 1	7 1	1

DL-L DL-R SL

OPERATION

FIG.36

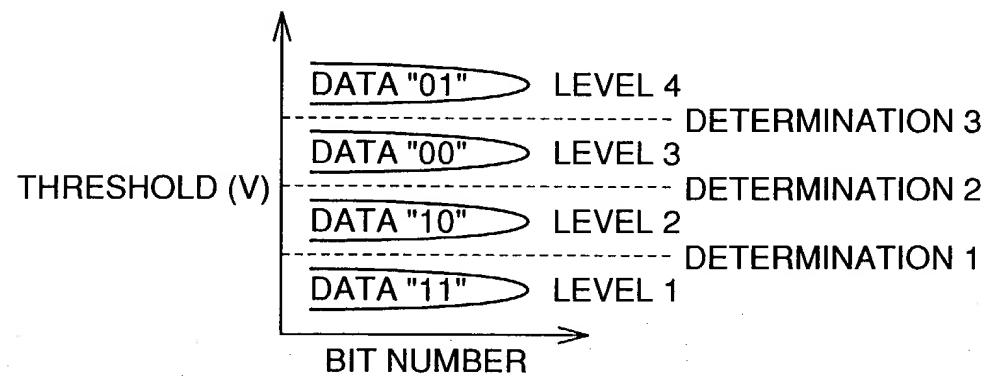




FIG. 37

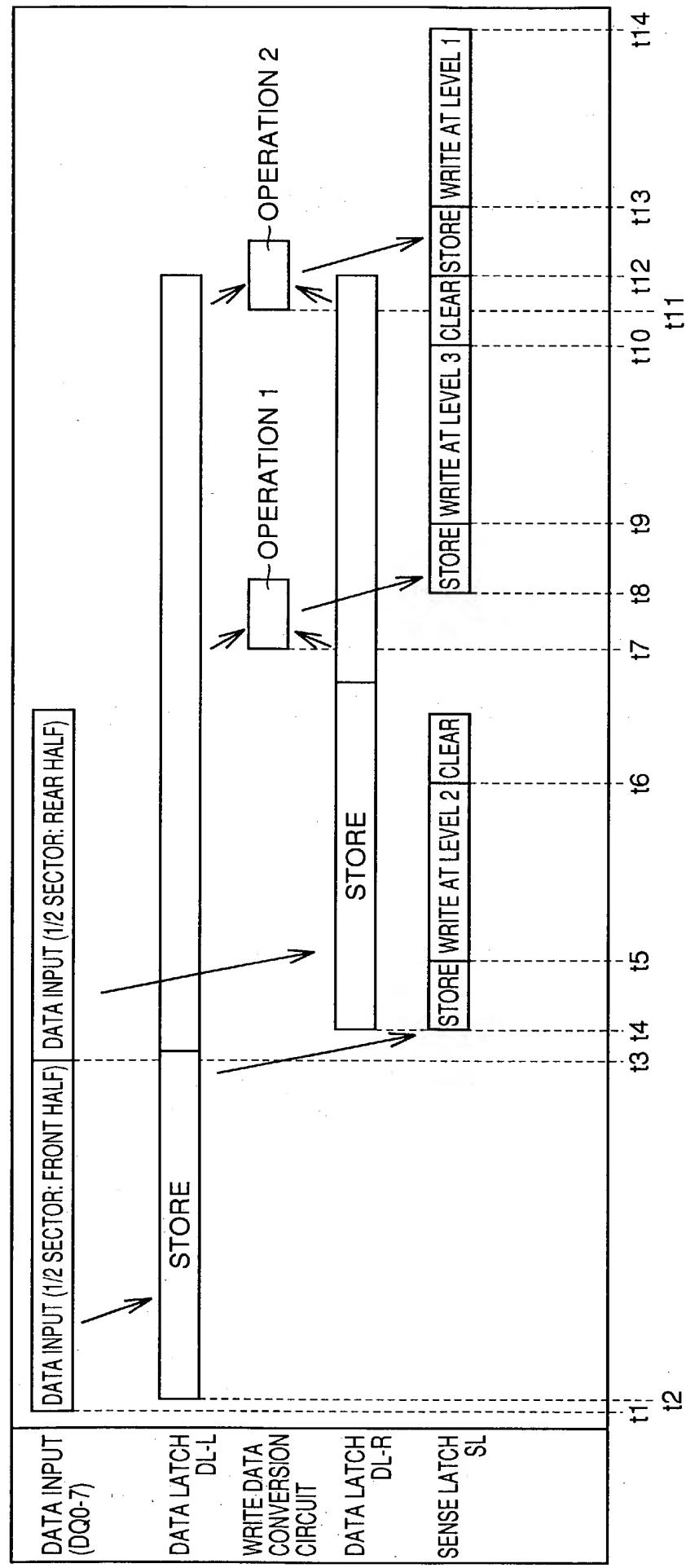




FIG.38

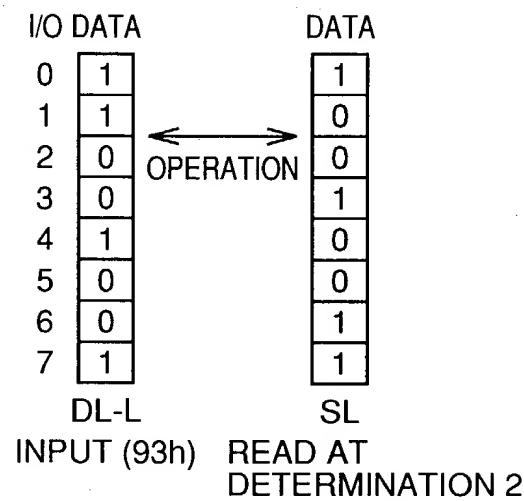


FIG. 39

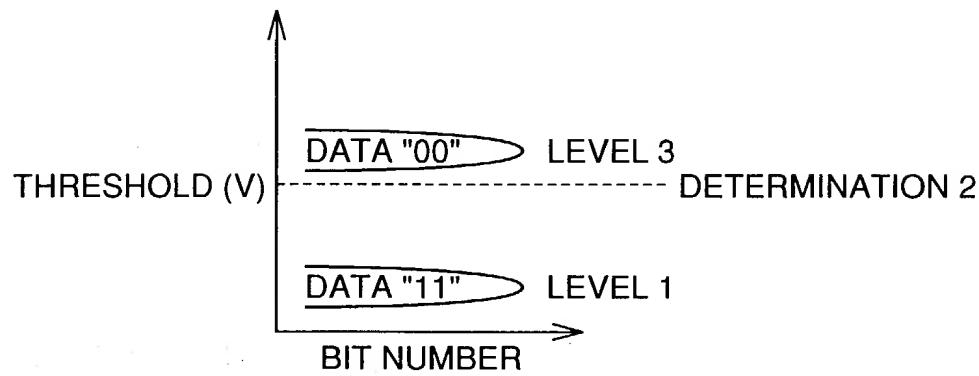




FIG.40

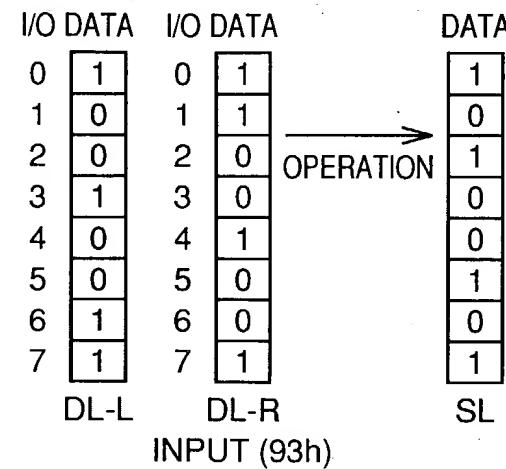


FIG.41

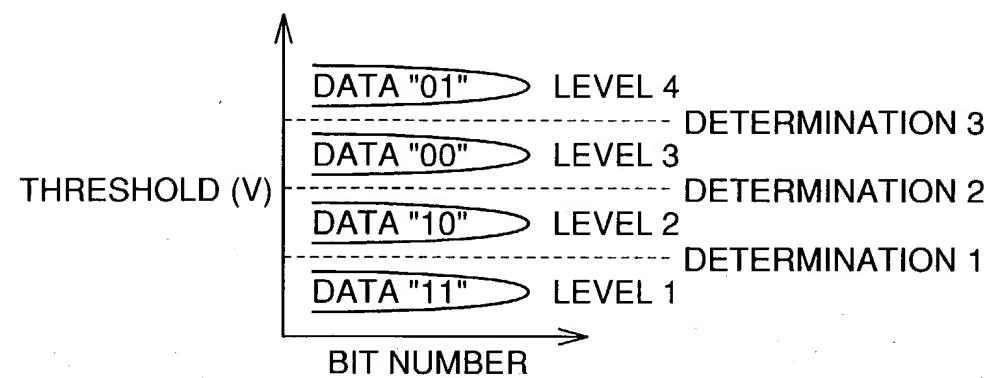
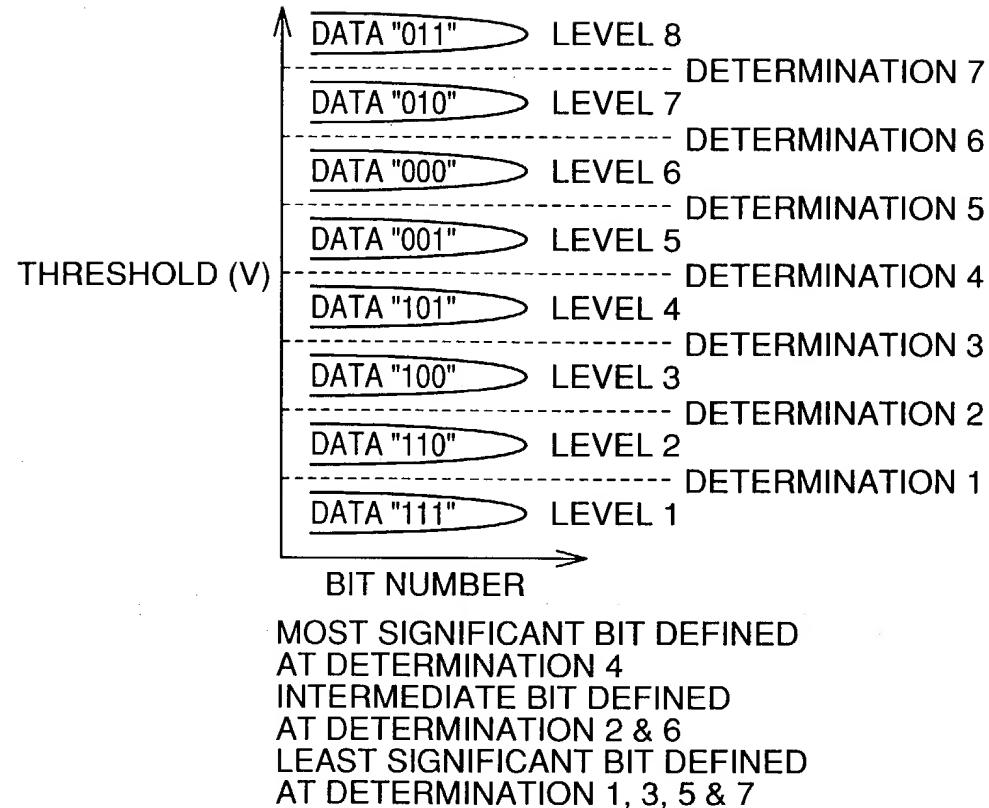




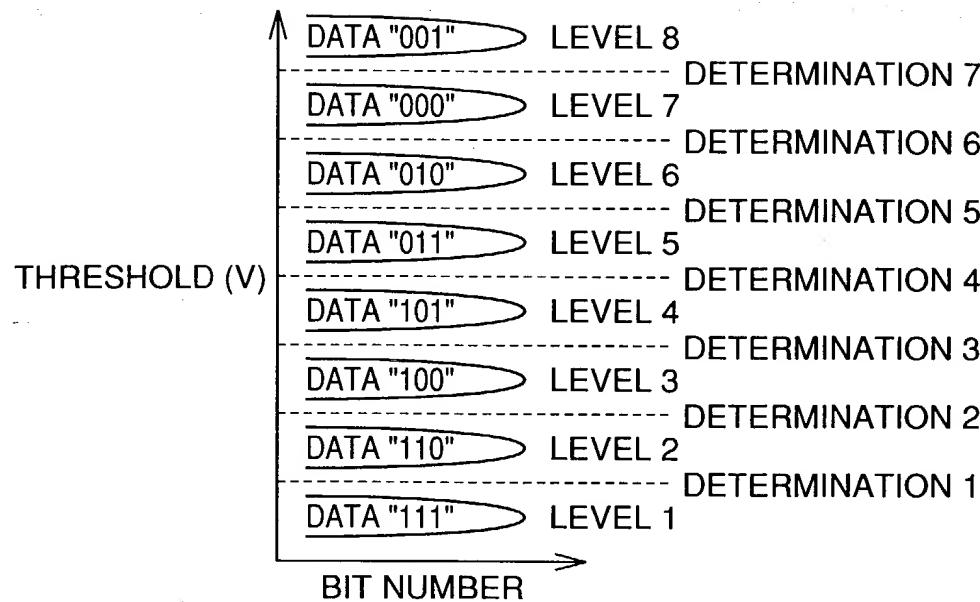
FIG.42



OK



FIG.43



MOST SIGNIFICANT BIT DEFINED
AT DETERMINATION 4
"0" & "1" AT LEVELS 3, 4, 5 & 6
AT DETERMINATION 2 & 6
NOT DEFINED
LEAST SIGNIFICANT BIT DEFINED
AT DETERMINATION 1, 3, 5 & 7

NG



FIG.44



FIG.45

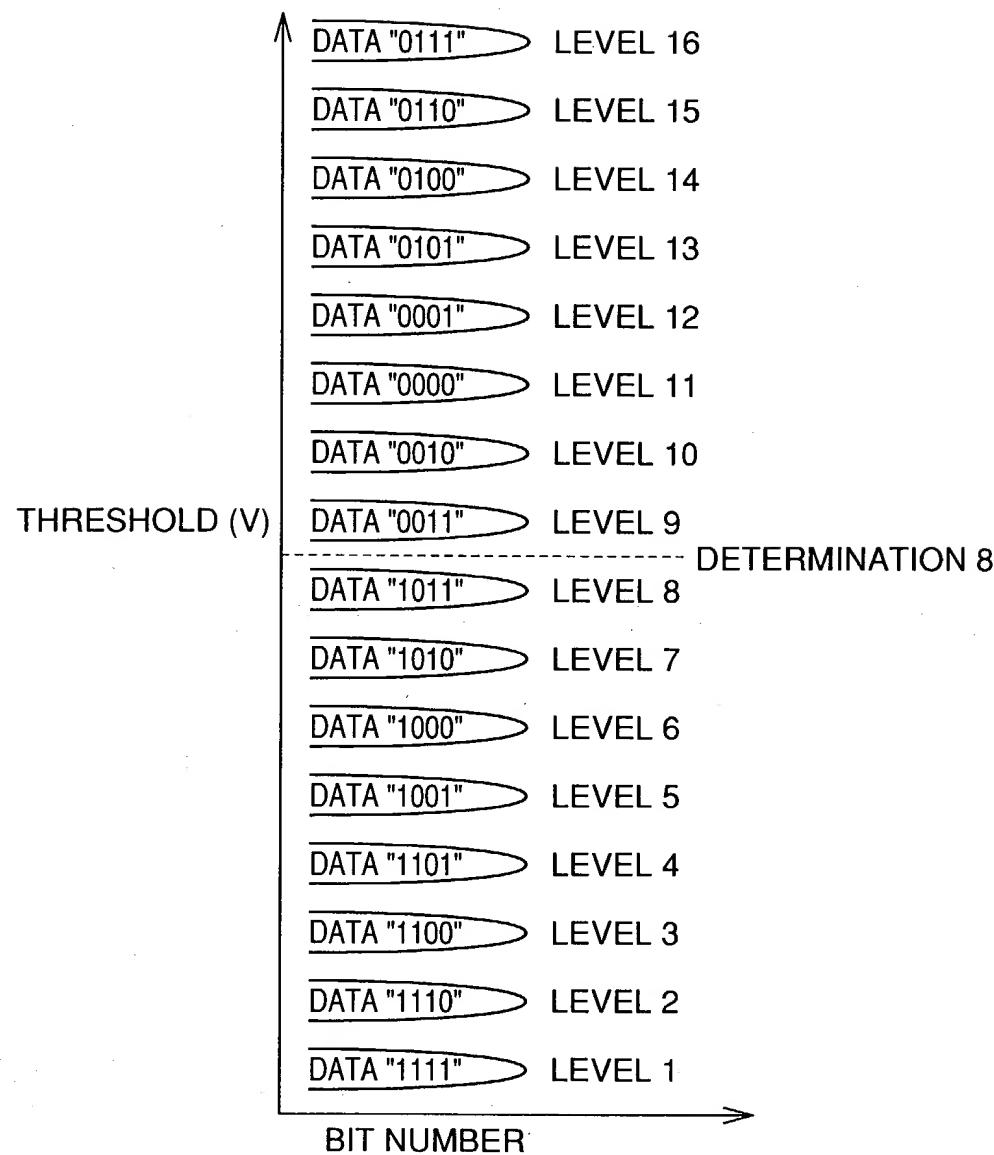




FIG.46

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	0	1	0	1
0	2	2	0	2
0	3	3	0	3
0	4	4	0	4
0	5	5	0	5
0	6	6	0	6
0	7	7	0	7
0	0	0	0	0
1	1	1	0	1
1	2	2	0	2
1	3	3	0	3
1	4	4	1	4
1	5	5	1	5
1	6	6	1	6
1	7	7	1	7
SL	DL-1	DL-2	DL-3	DL-4
		OUTPUT (00h-FFh)		



FIG.47

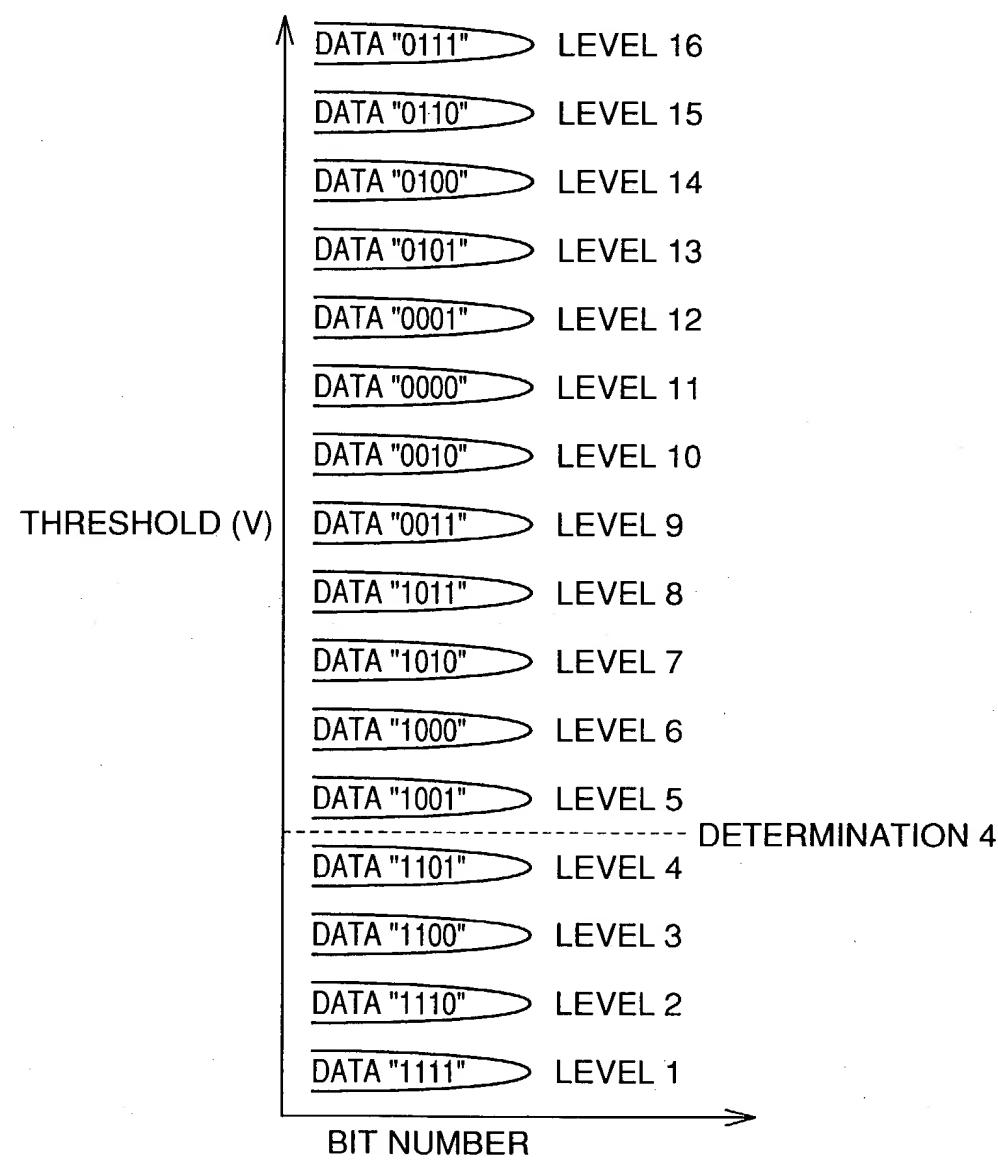




FIG.48

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	0	1	1
0	2	0	2	2
0	3	0	3	3
1	4	0	4	4
1	5	0	5	5
1	6	0	6	6
1	7	0	7	7
1	0	1	0	0
1	1	1	1	1
1	2	1	2	2
1	3	1	3	3
1	4	1	4	4
1	5	1	5	5
1	6	1	6	6
1	7	1	7	7
SL	DL-1	DL-2	DL-3	DL-4
	OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)		



FIG.49

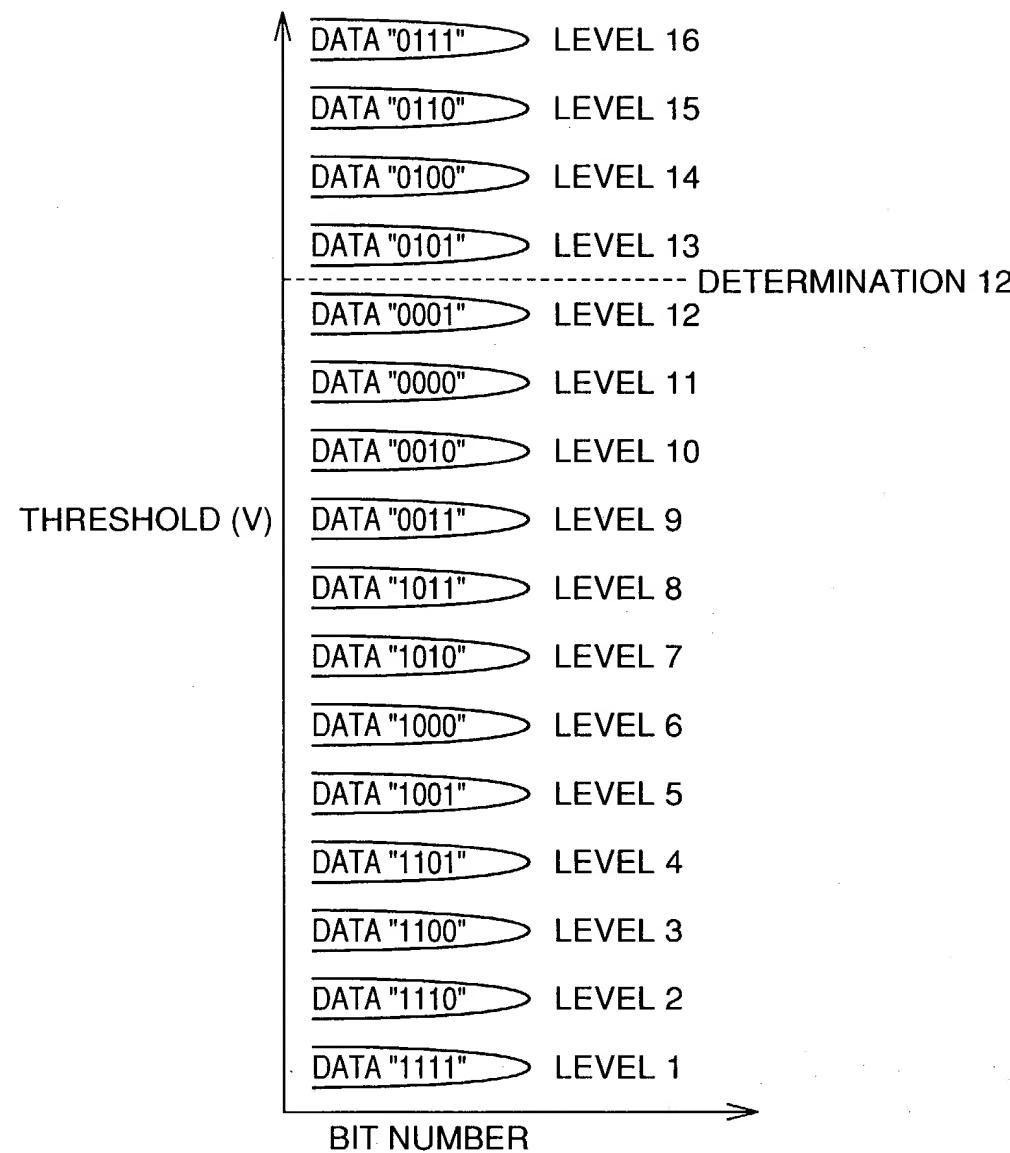




FIG.50

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	
0	0	0	0	0	0
0	1	0	1	0	1
0	2	0	2	0	2
0	3	0	3	0	3
0	4	0	4	1	4
0	5	0	5	1	5
0	6	0	6	1	6
0	7	0	7	1	7
0	0	1	0	1	0
0	1	1	1	1	1
0	2	1	2	1	2
0	3	1	3	1	3
0	4	1	4	0	4
0	5	1	5	0	5
1	6	1	6	0	6
1	7	1	7	0	7
SL	DL-1	DL-2	DL-3	DL-4	
	OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)			



FIG.51

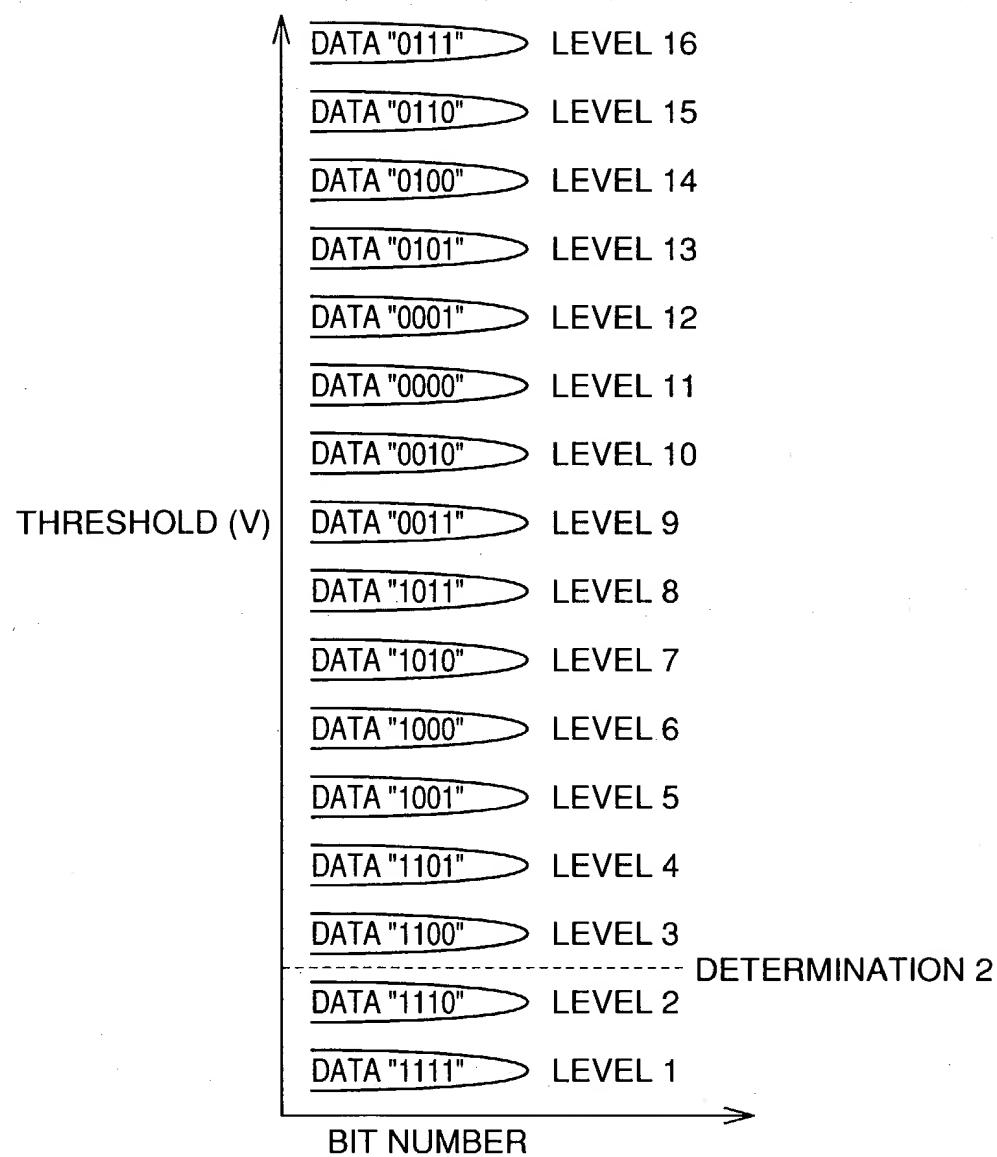




FIG.52

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	
0	0	0	0	0	0
0	1	0	1	0	1
0	2	0	2	0	2
NOR WITH INVERTED DATA OF SL TO DL-3		3	0	3	3
0	4	1	4	0	4
0	5	0	5	0	5
0	6	0	6	0	6
0	7	0	7	0	7
0	0	1	0	0	0
0	1	1	1	0	1
1	2	1	2	1	2
1	3	1	3	1	3
1	4	1	4	1	4
1	5	1	5	0	5
1	6	1	6	0	6
1	7	1	7	0	7
SL	DL-1	DL-2	DL-3	DL-4	
	OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)			



FIG.53

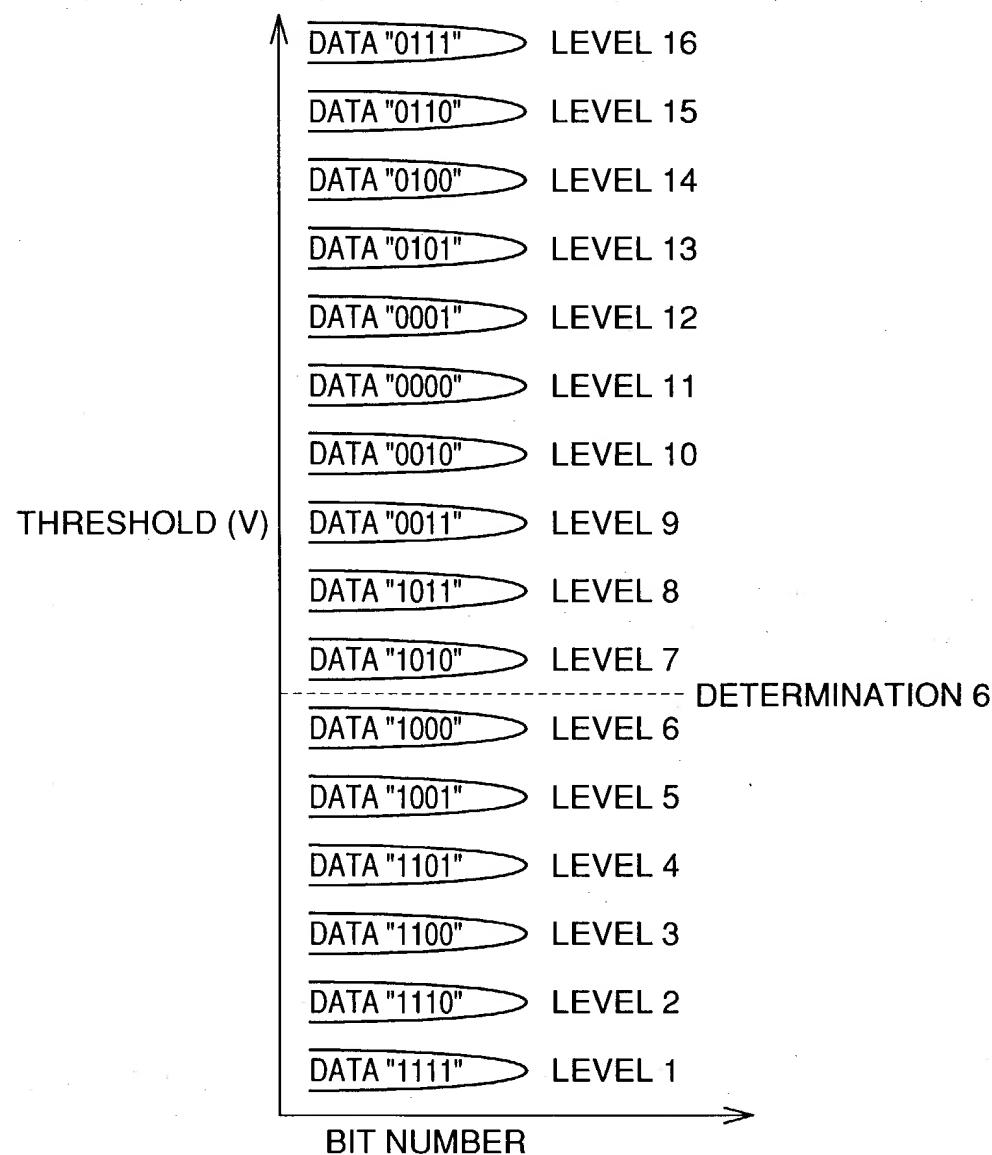




FIG.54

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0	0
0	1	0	1	0	1
0	2	0	2	0	2
0	3	0	3	0	3
0	4	0	4	1	4
0	5	0	5	1	5
1	6	0	6	1	6
1	7	0	7	1	7
1	0	1	0	1	0
1	1	1	1	0	1
1	2	1	2	1	2
1	3	1	3	1	3
1	4	1	4	0	4
1	5	1	5	0	5
1	6	1	6	0	6
1	7	1	7	0	7
SL	DL-1	DL-2	DL-3	DL-4	
	OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)			



FIG.55

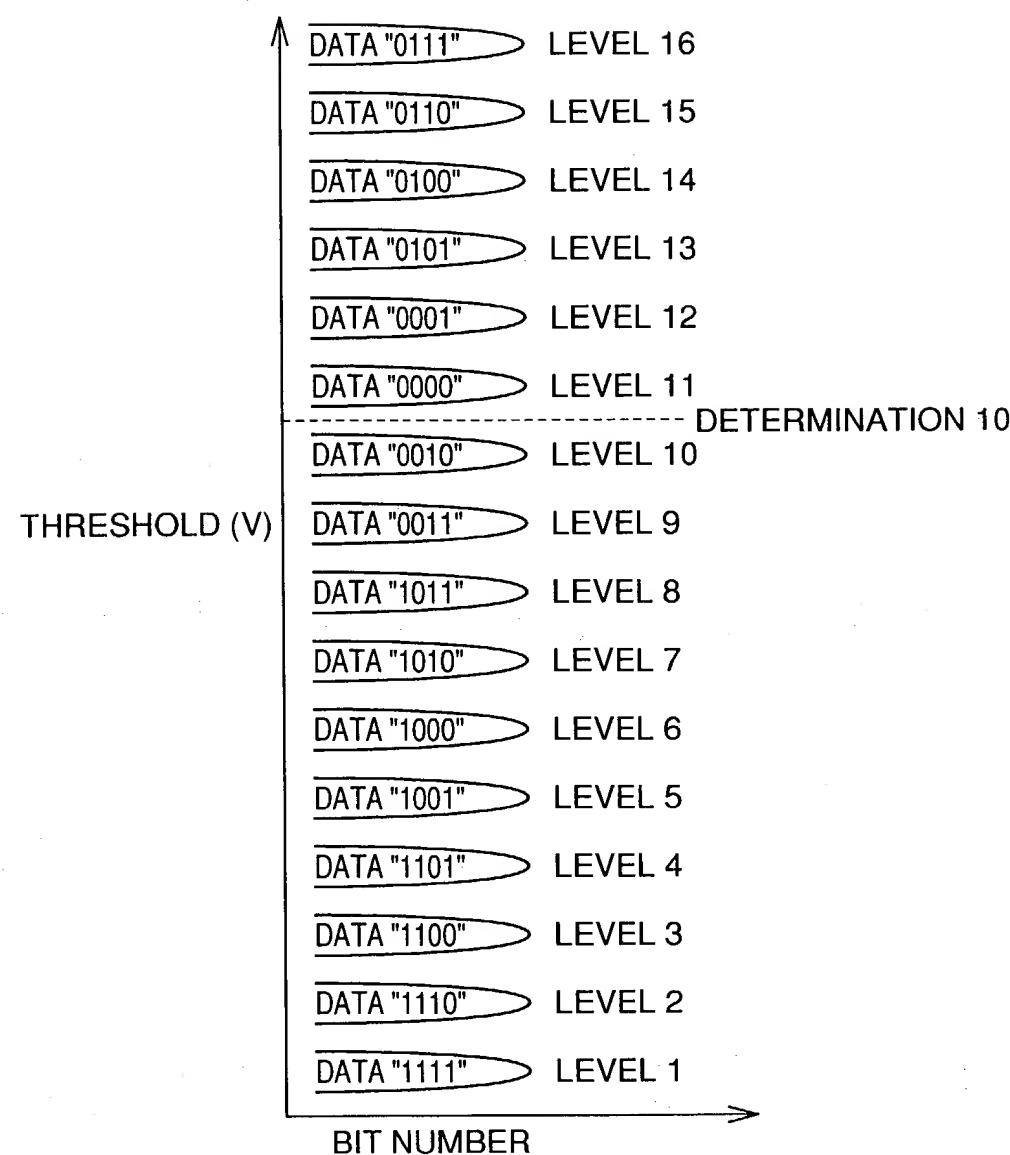




FIG.56

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	1	1	1
1	2	2	2	2
NOR	0	0	0	0
1	3	3	3	3
INVERTED	0	0	0	1
1	4	4	4	4
DATA OF SL	0	1	0	1
1	5	5	5	5
AND DATA	0	1	0	1
OF DL-4	6	6	6	6
1	7	7	7	7
TO DL-4	0	1	0	0
1	1	1	1	0
1	2	2	2	1
1	3	3	3	1
1	4	4	4	1
1	5	5	5	1
1	6	6	6	0
1	7	7	7	0
SL	DL-1	DL-2	DL-3	DL-4
OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)			



FIG.57

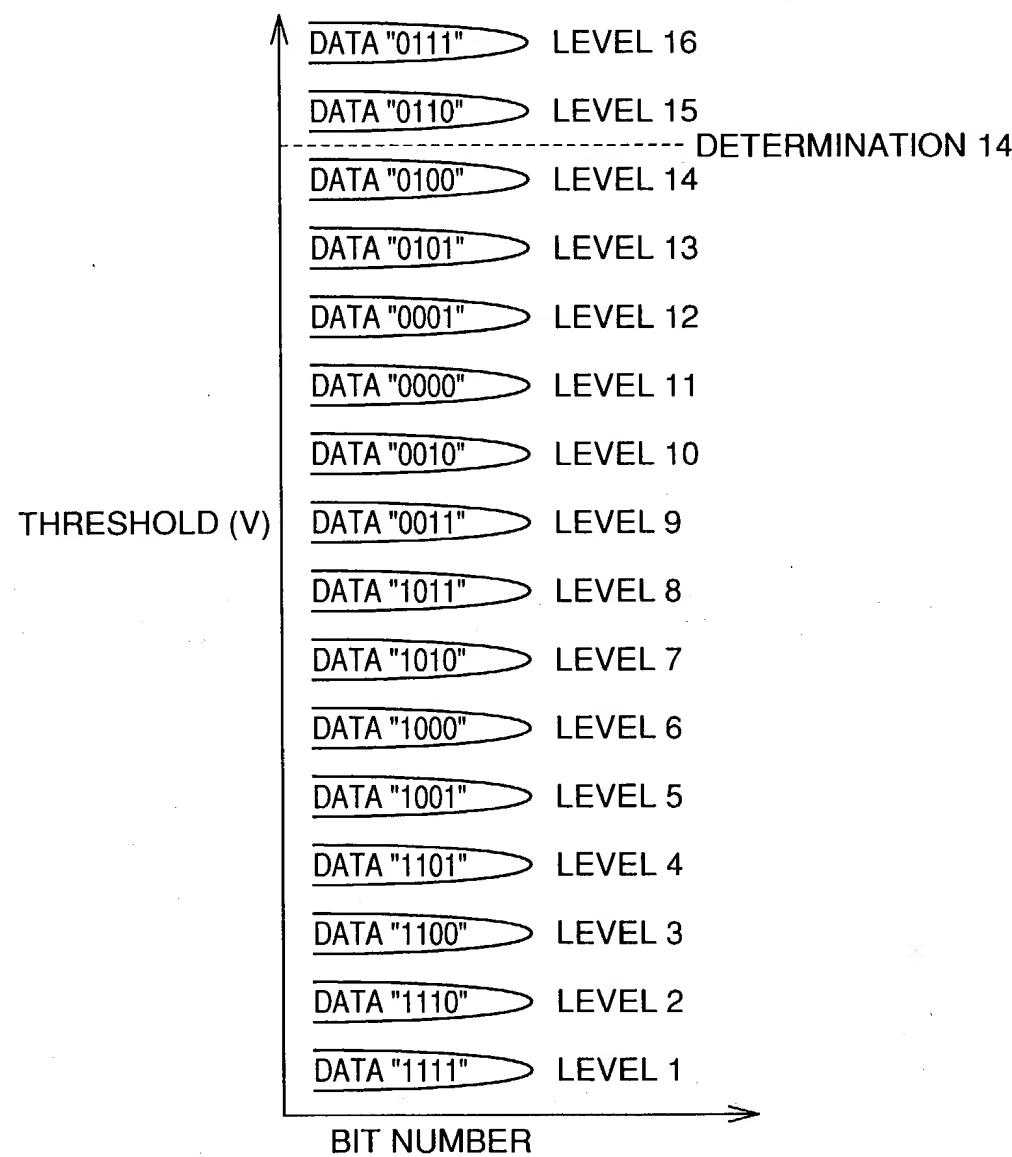




FIG.58

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	
	0 0	0 0	0 0	0 0	
	1 0	1 0	1 0	1 0	
	2 0	2 0	2 1	2 1	
	3 0	3 0	3 1	3 1	
	4 0	4 1	4 1	4 1	
	5 0	5 1	5 1	5 1	
	6 0	6 1	6 0	6 0	
	7 0	7 1	7 0	7 0	
0	0 1	0 1	0 0	0 0	
1	1 1	1 1	1 0	1 0	
2	1 1	2 1	2 1	2 1	
3	1 1	3 1	3 1	3 1	
4	1 1	4 0	4 1	4 1	
5	1 1	5 0	5 1	5 1	
6	1 1	6 0	6 0	6 0	
7	1 1	7 0	7 0	7 0	
SL	DL-1	DL-2	DL-3	DL-4	
OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1	OR DATA OF DL-3 AND DL-4 AND STORE RESULT IN DL-3 (0Fh-F0h)			



FIG.59

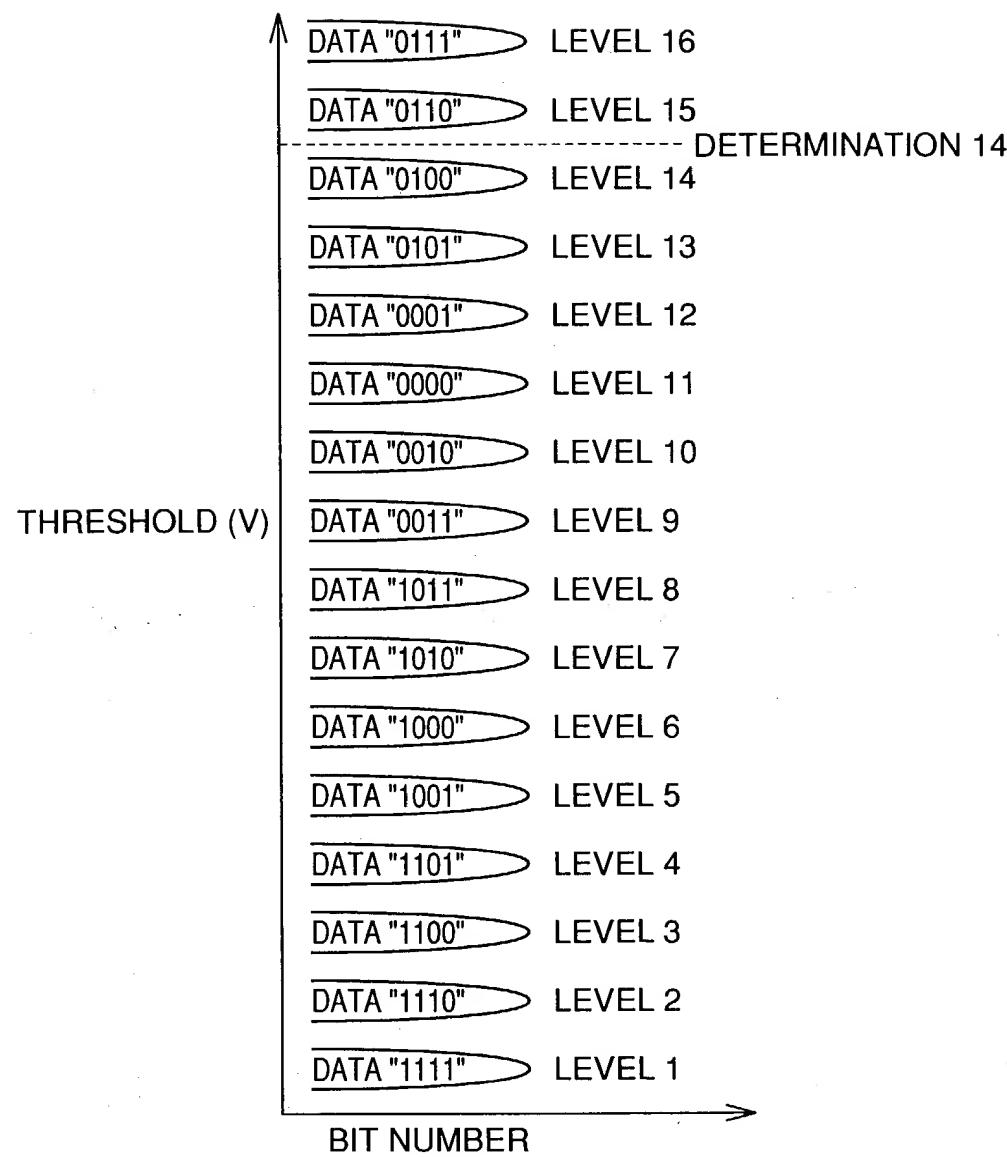




FIG.60

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	0	1	0
0	2	0	2	1
0	3	0	3	1
0	4	1	4	1
0	5	1	5	1
0	6	1	6	0
0	7	1	7	0
0	0	1	0	0
0	1	1	1	0
0	2	1	2	1
0	3	1	3	1
0	4	0	4	1
0	5	0	5	1
0	6	0	6	0
1	7	0	7	0

SL → TO DL-4

DL-1 DL-2 DL-3 DL-4

OUTPUT (0Fh-F0h) OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)



FIG.61

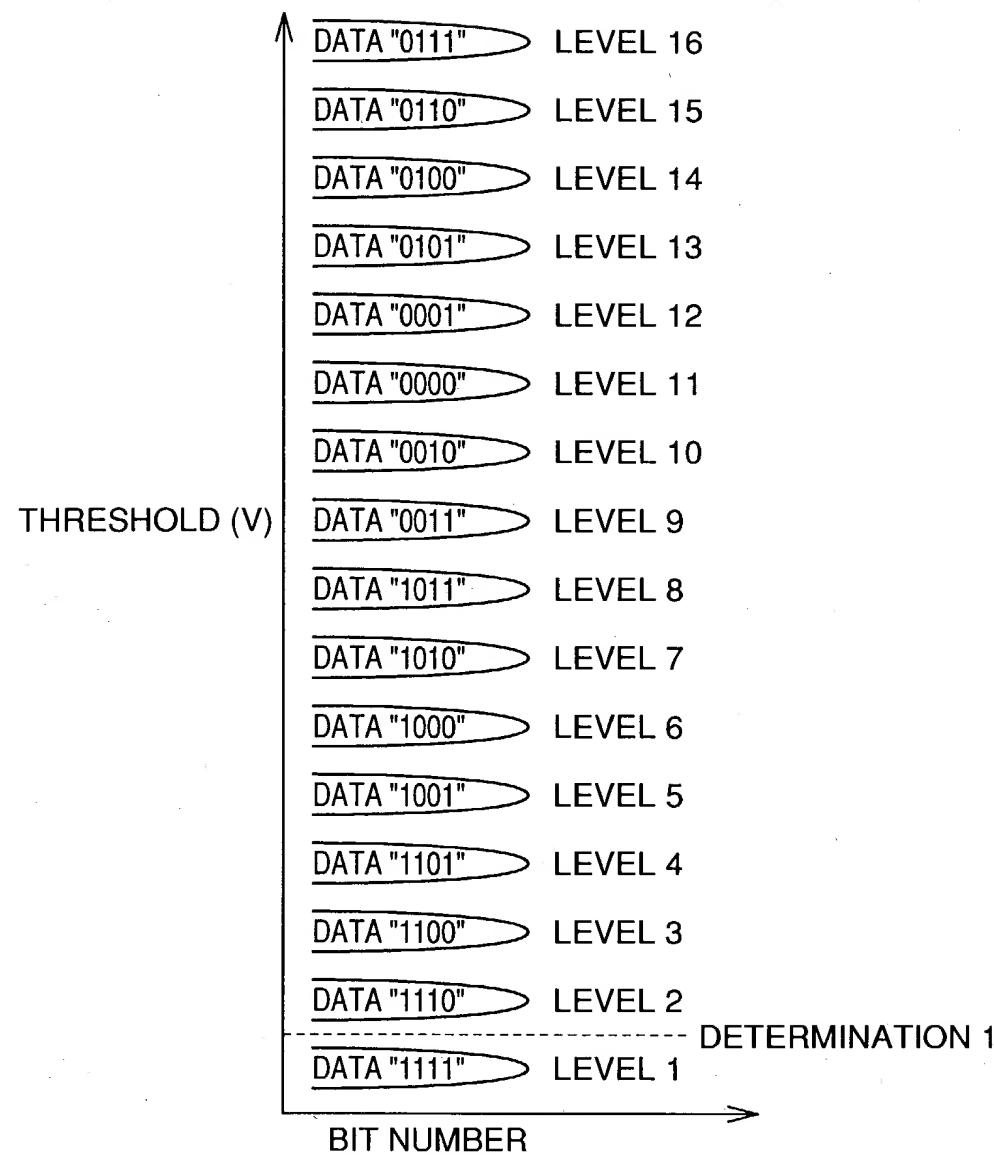




FIG.62

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	0	1	0
0	2	0	2	1
NOR	2	0	2	0
0	3	0	3	1
INVERTED	3	0	3	0
0	4	1	4	1
DATA OF SL	4	1	4	0
0	5	1	5	1
AND DATA	5	1	5	0
0	6	1	6	0
OF DL-4	6	1	6	0
0	7	1	7	0
TO DL-4	7	1	7	0
0	0	0	0	0
0	1	1	1	0
0	2	1	2	1
0	3	1	3	1
0	4	0	4	1
1	5	0	5	1
1	6	0	6	1
1	7	0	7	0
SL	DL-1	DL-2	DL-3	DL-4
			OUTPUT (00h-FFh)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)



FIG.63

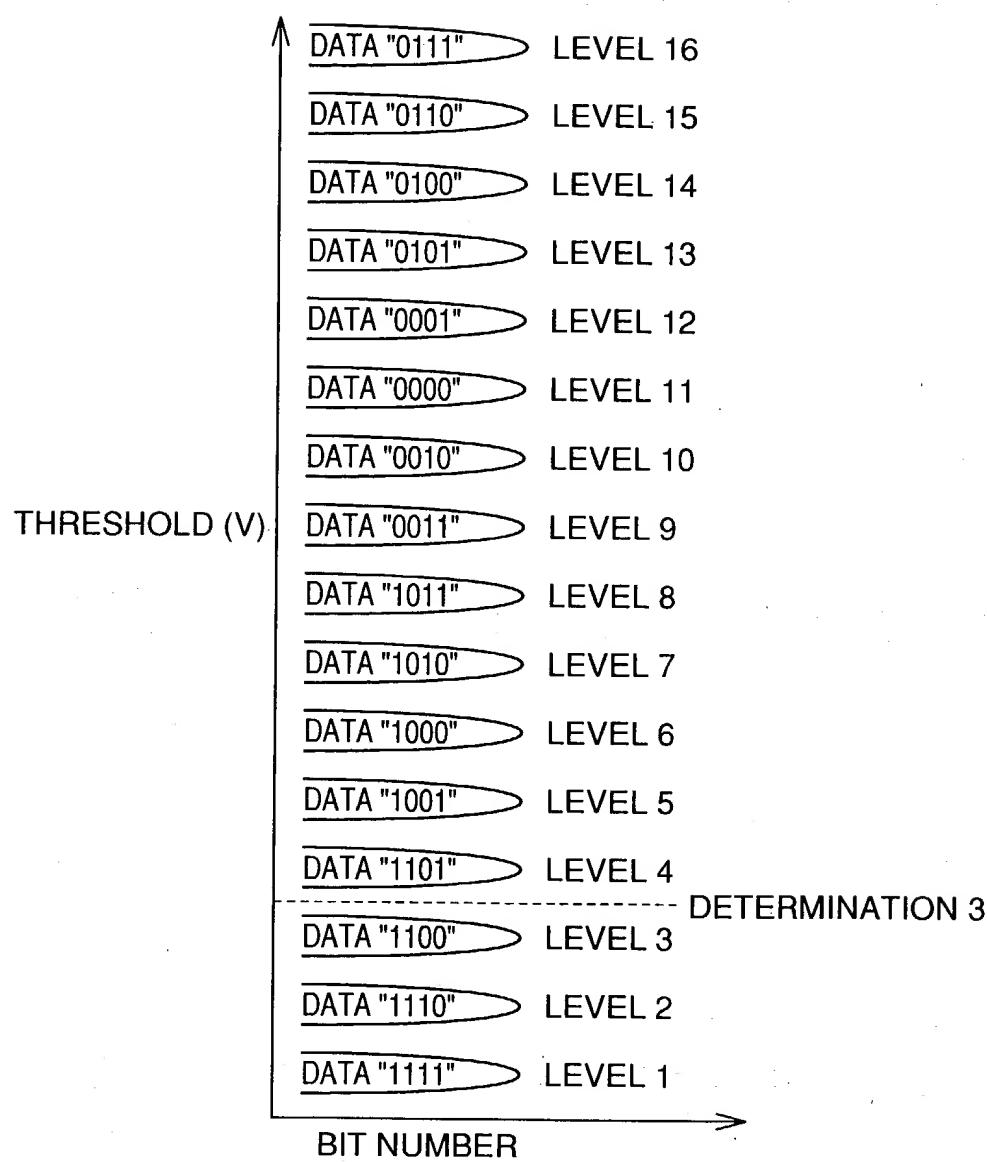




FIG.64

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	1	1	1
0	2	2	2	2
0	3	3	3	3
0	4	4	4	4
0	5	5	5	5
0	6	6	6	6
0	7	7	7	7
0	0	0	0	0
0	1	1	1	1
0	2	2	2	2
1	3	3	3	3
1	4	4	4	4
1	5	5	5	5
1	6	6	6	6
1	7	7	7	7

SL → TO DL-1

DL-1 DL-2 DL-3 DL-4

OUTPUT (0Fh-F0h) OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)



FIG.65

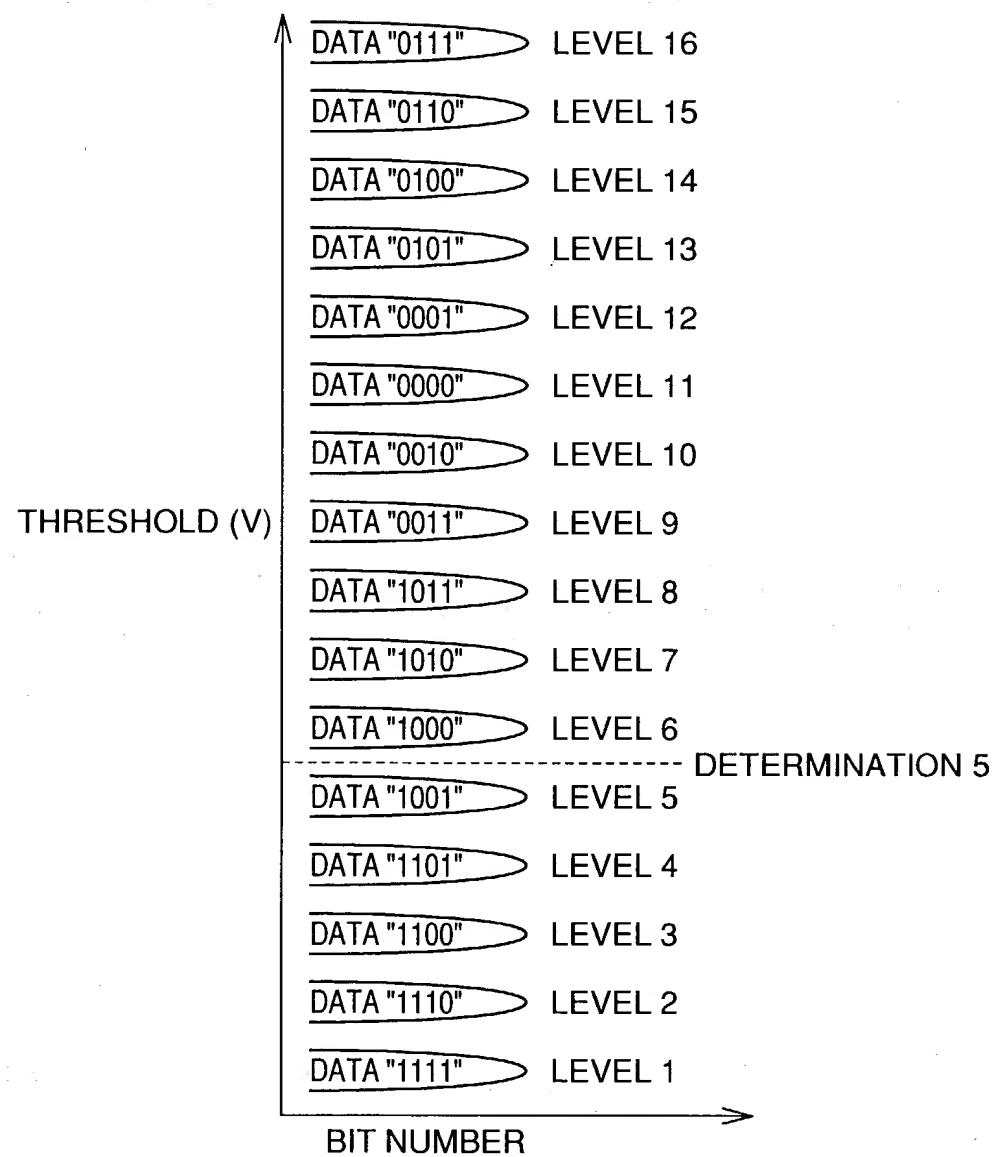




FIG.66

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	0	1	0
0	NOR	2	0	2
0	INVERTED	3	0	3
0	DATA OF SL	4	1	4
0	AND DATA	5	1	5
0	OF DL-1	6	0	6
0	TO DL-1	7	0	7
0		0	0	0
1		1	0	1
1		2	1	2
1		3	0	3
1		4	0	4
1		5	0	5
1		6	0	6
1		7	0	7
SL	DL-1	DL-2	DL-3	DL-4
	OUTPUT (00h-FFh)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)		



FIG.67

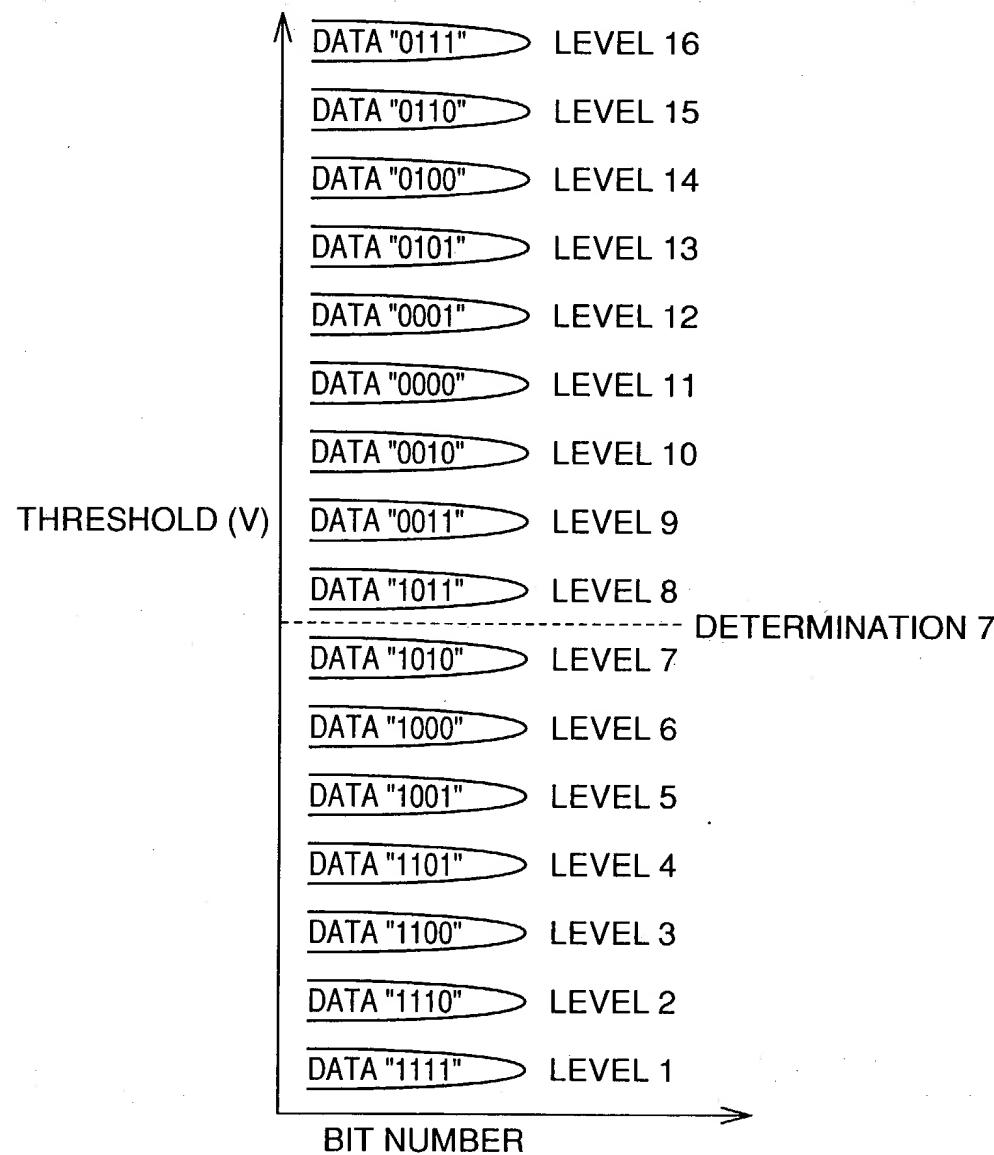




FIG.68

OR DATA OF
DL-1 AND DL-4
TO DL-4

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
	0 0	0 0	0 0	0 0
	1 0	1 0	1 0	1 0
	2 0	2 0	2 1	2 0
	3 0	3 0	3 1	3 0
	4 0	4 1	4 1	4 0
	5 0	5 1	5 1	5 0
	6 0	6 1	6 0	6 0
	7 0	7 1	7 0	7 0
SL	0 0	0 1	0 0	0 0
	1 1	1 1	1 0	1 1
	2 1	2 1	2 1	2 1
	3 0	3 1	3 1	3 0
	4 0	4 0	4 1	4 0
	5 0	5 0	5 1	5 1
	6 0	6 0	6 0	6 1
	7 0	7 0	7 0	7 0
	DL-1	DL-2	DL-3	DL-4
OUTPUT (0Fh-F0h)	OUTPUT (0Fh-F0h)	INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)		



FIG.69

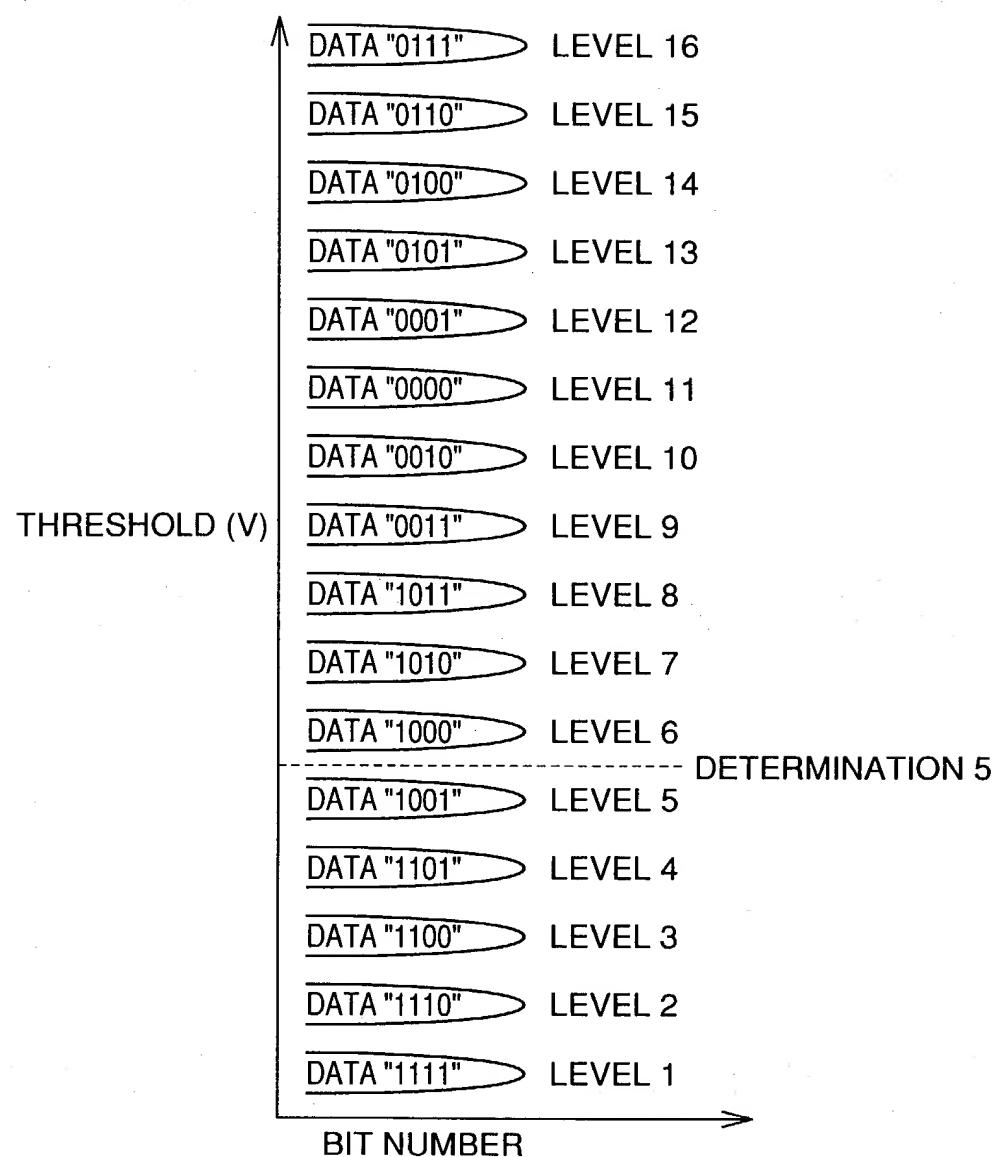




FIG. 70

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	0	1	0	1
0	2	2	0	2
0	3	3	0	3
0	4	4	1	4
0	5	5	1	5
0	6	6	1	6
1	7	7	1	7
1	0	0	1	0
1	1	1	1	0
1	2	2	1	1
1	3	3	1	3
1	4	4	0	4
1	5	5	0	5
1	6	6	0	6
1	7	7	0	7
SL	DL-1	DL-2	DL-3	DL-4
	OUTPUT (00h-FFh)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)		



FIG.71

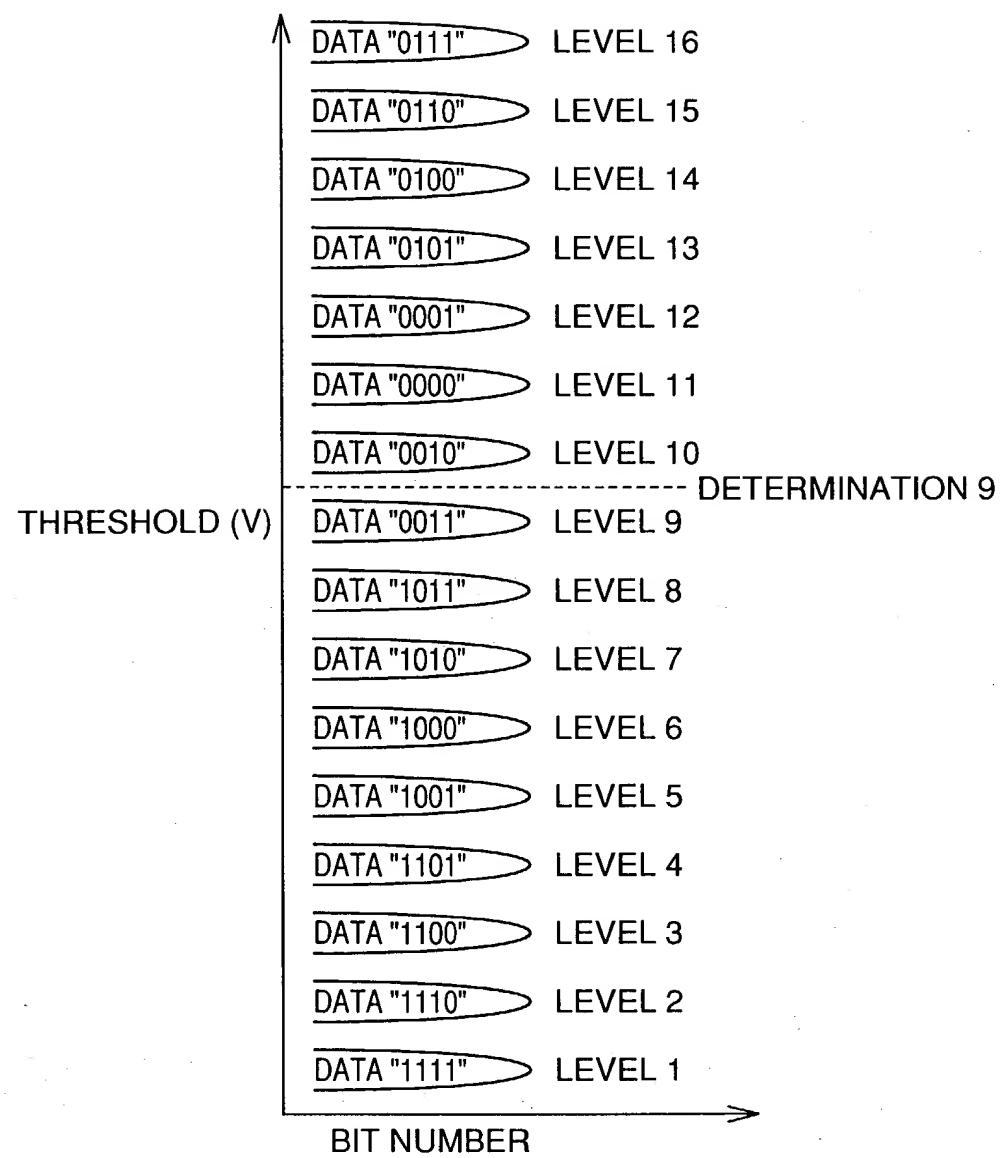




FIG. 72



FIG.73

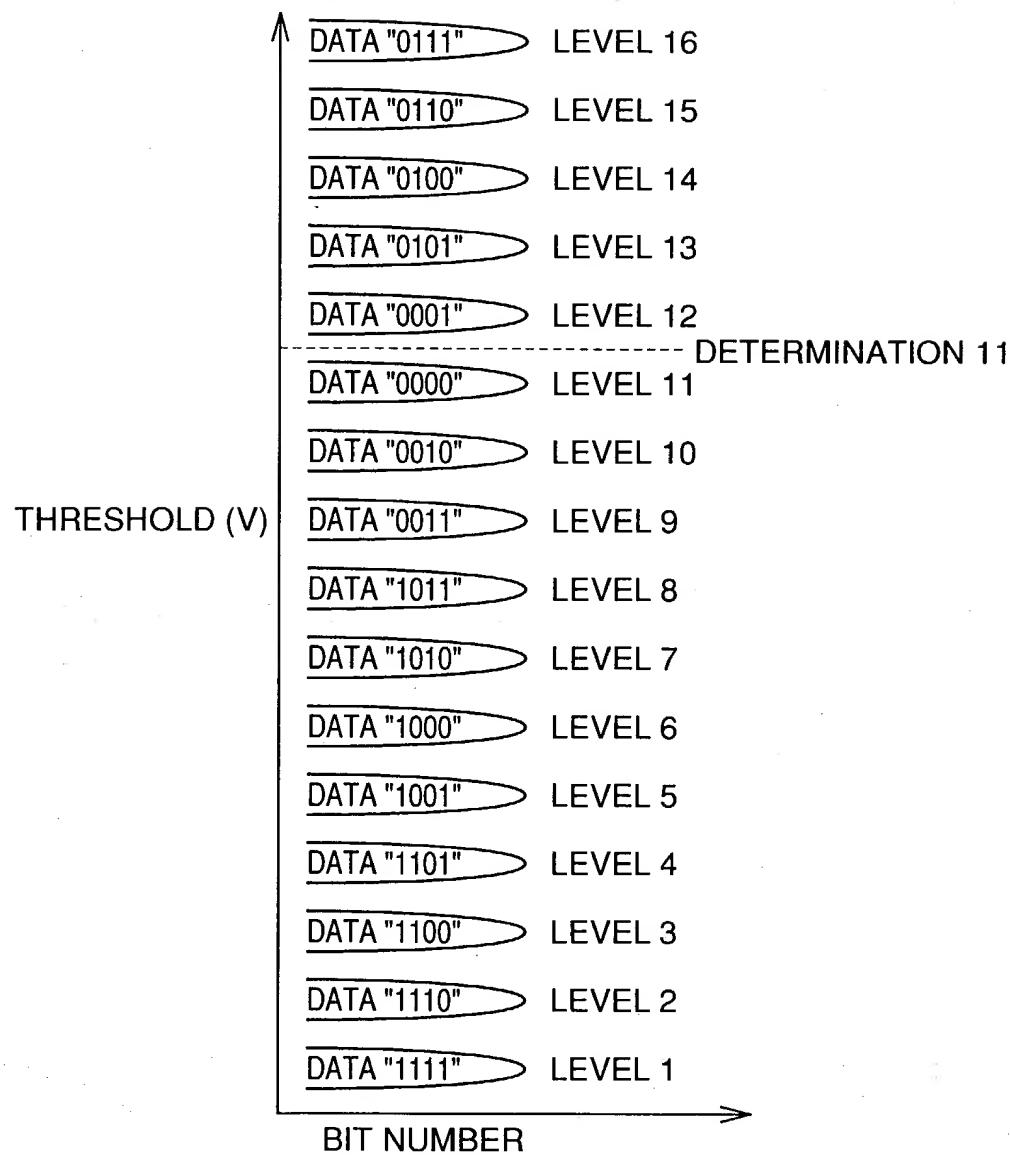




FIG.74

OR DATA OF DL-1 AND DL-4
TO DL-4

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
	0	0	0	0
	1	0	1	0
	2	0	2	0
	3	0	3	0
	4	0	4	1
	5	1	5	1
	6	1	6	1
	7	0	7	1
SL	0	0	0	0
	1	0	1	1
	2	0	2	1
	3	0	3	1
	4	0	4	0
	5	0	5	1
	6	0	6	0
	7	0	7	0
	DL-1	DL-2	DL-3	DL-4
	OUTPUT (0Fh-F0h)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)		



FIG.75

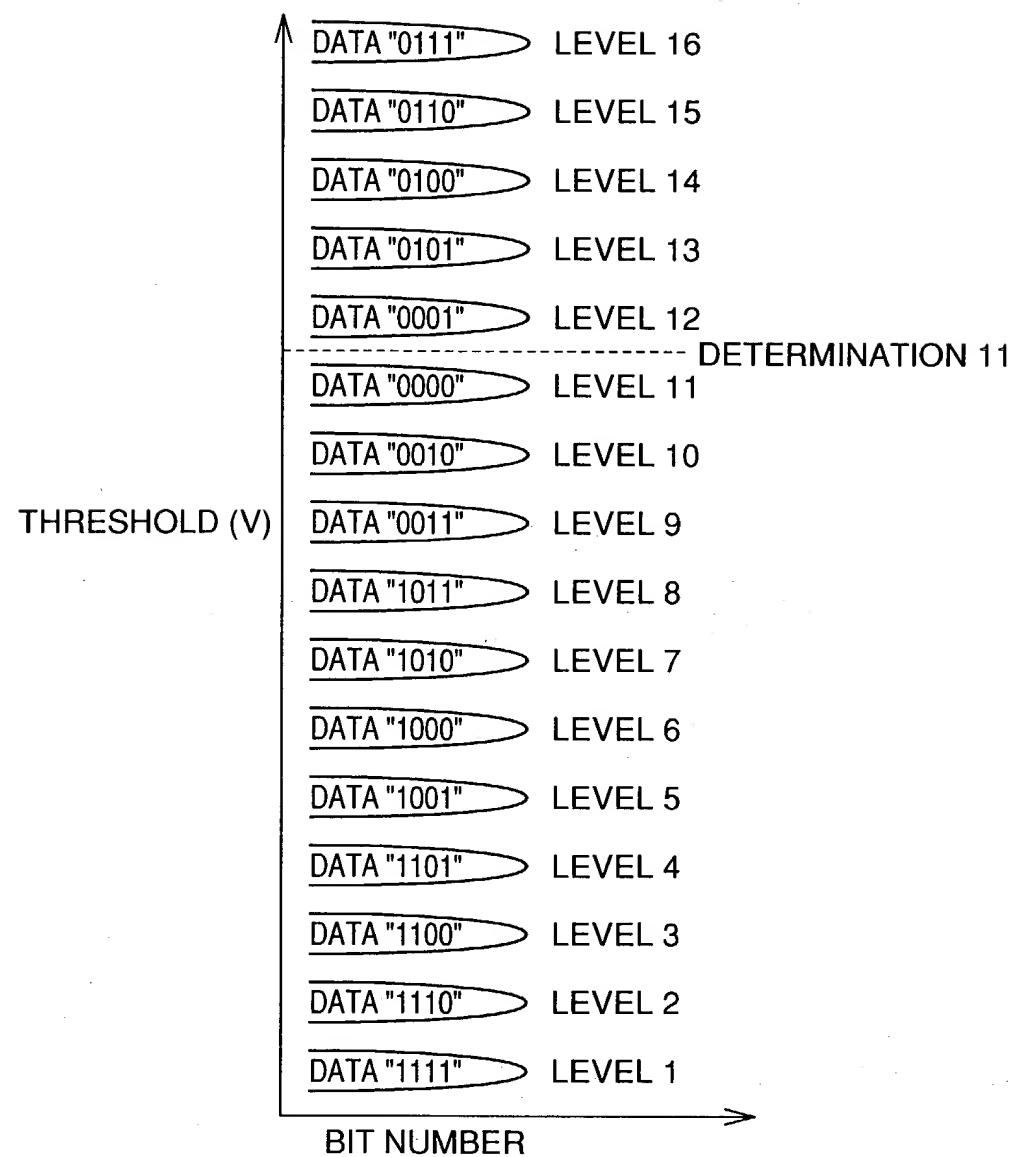




FIG.76

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
0	1	0	1	0
0	2	0	2	1
1	3	1	3	0
1	4	1	4	1
1	5	1	5	1
1	6	1	6	0
1	7	1	7	0
1	0	1	0	0
1	1	1	1	0
1	2	1	2	1
1	3	1	3	1
1	4	1	4	0
1	5	1	5	0
1	6	1	6	0
1	7	1	7	0

SL → TO DL-1

DL-1 DL-2 DL-3 DL-4

OUTPUT (00h-FFh) OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)



FIG.77

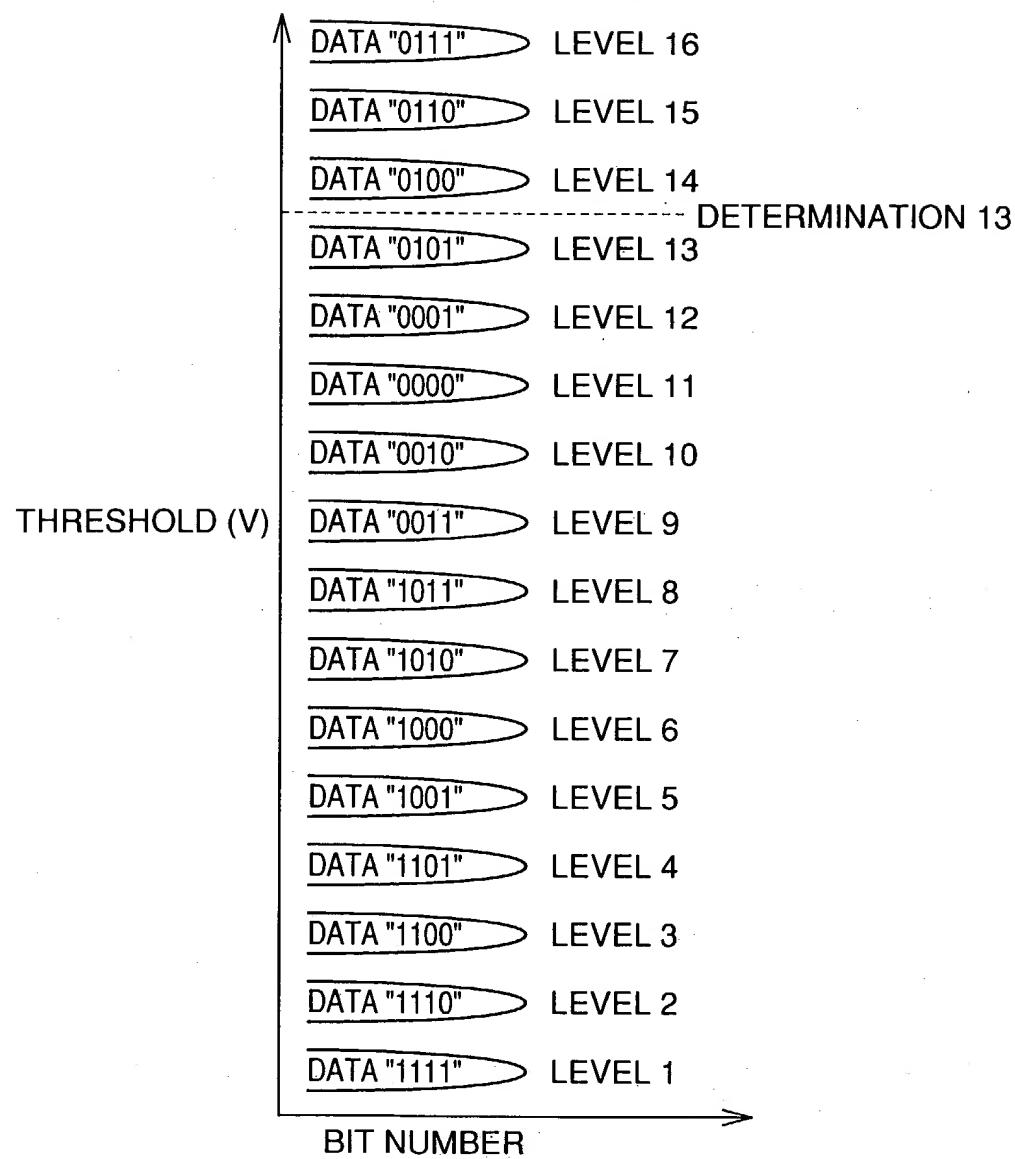




FIG.78

OR DATA OF DL-1 AND DL-4
TO DL-4

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0	0	0
1	1	1	1	1
1	NOR	2	1	2
1	INVERTED	3	0	3
1	DATA OF SL	4	0	4
1	AND DATA	5	0	5
1	OF DL-1	6	0	6
1	TO DL-1	7	0	7
1		0	1	0
1		1	1	1
1		2	1	2
1		3	1	3
1		4	0	4
1		5	0	5
1		6	0	6
1		7	0	7
SL	DL-1	DL-2	DL-3	DL-4
		OUTPUT (0Fh-F0h)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)	



FIG.79

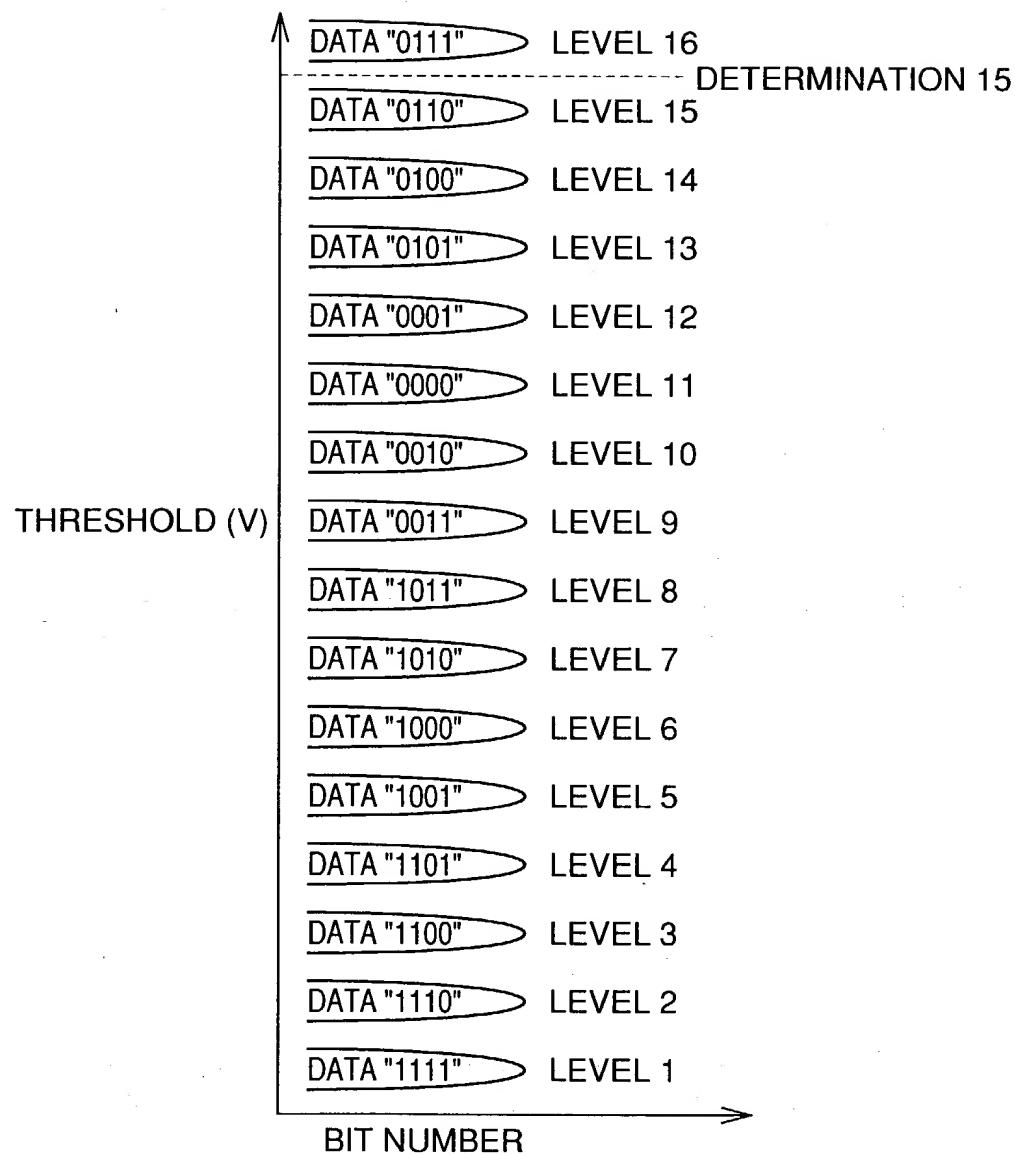




FIG.80

OR DATA OF DL-1 AND DL-4
TO DL-4

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
	0	0	0	0
	1	1	1	0
OR DATA OF DL-1 AND DL-4 TO DL-4	2	1	2	0
	3	0	3	0
	4	0	4	1
	5	0	5	1
	6	0	6	1
	7	0	7	1
	0	0	0	1
	1	0	1	1
	2	0	2	1
	3	0	3	1
	4	0	4	0
	5	0	5	0
	6	0	6	0
	7	0	7	0
SL	DL-1	DL-2	DL-3	DL-4
	OUTPUT (0Fh-F0h)	OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)		



FIG.81

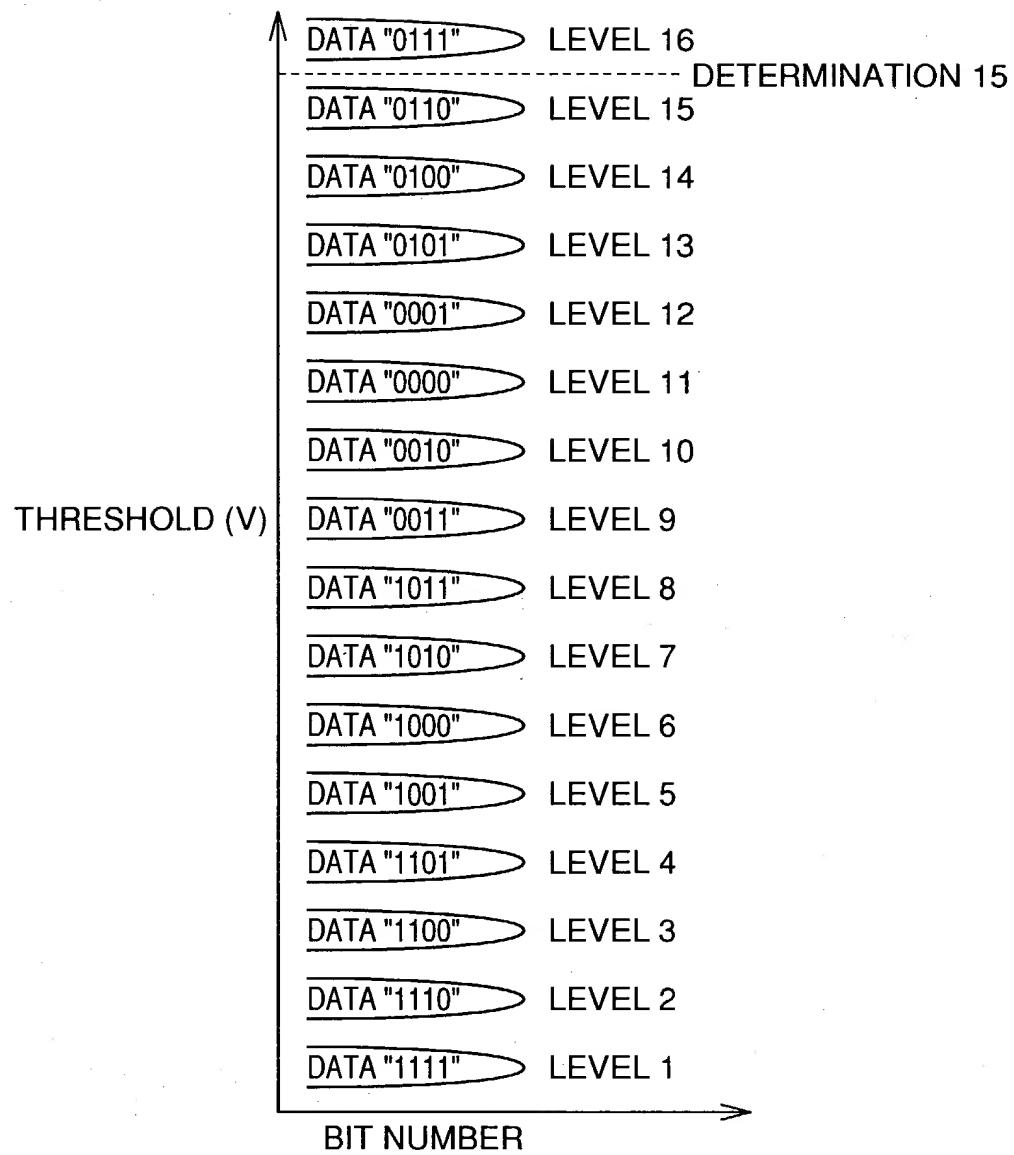




FIG.82

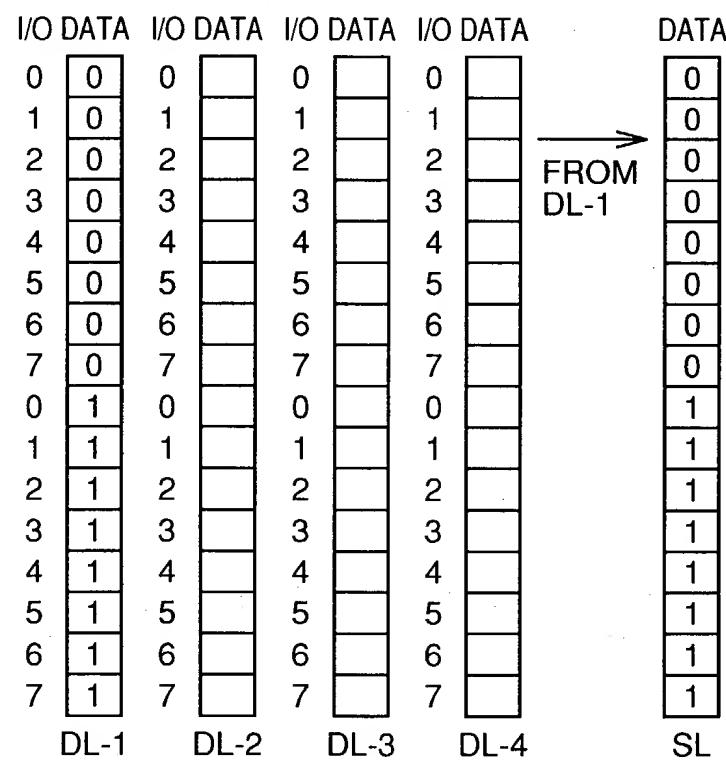




FIG.83

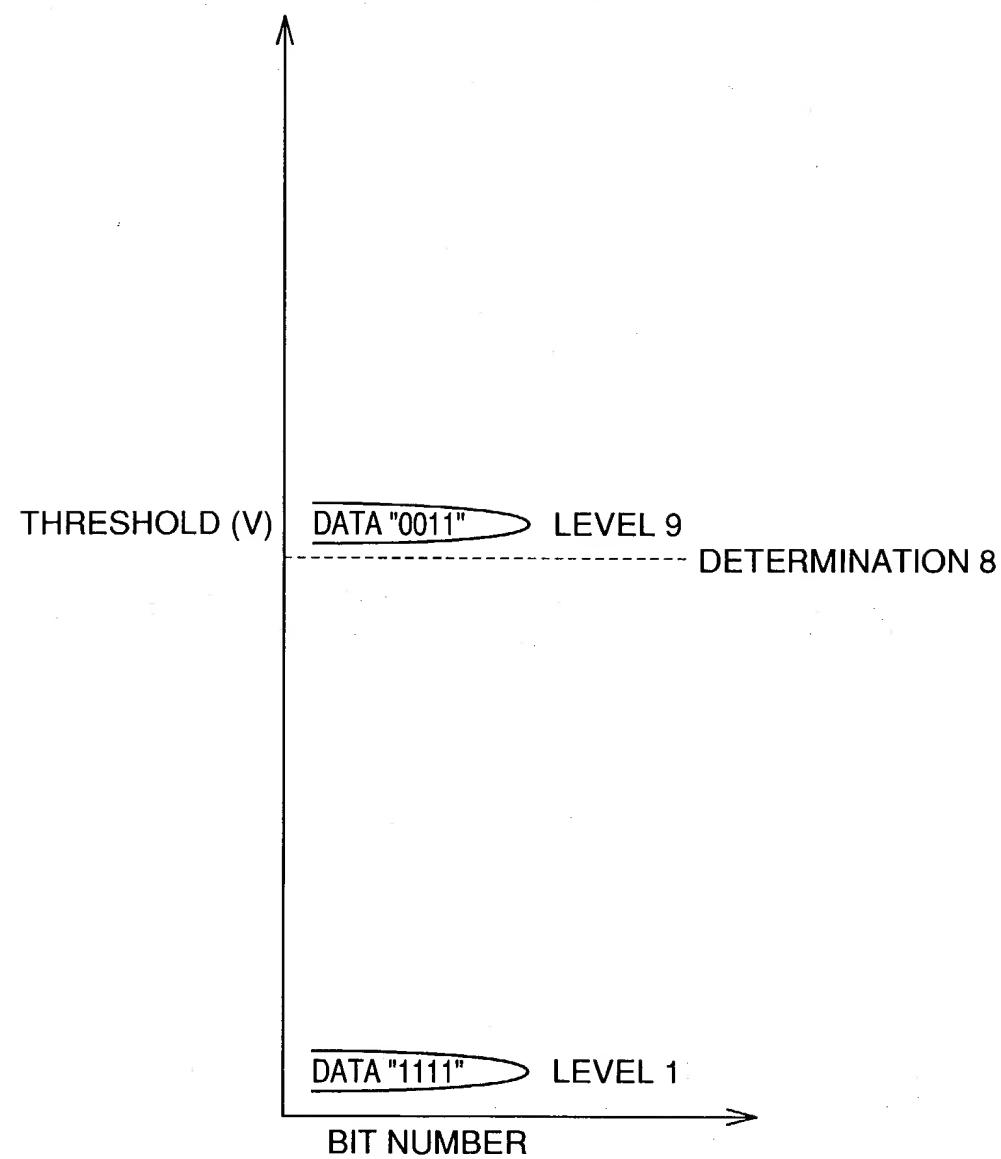




FIG. 84

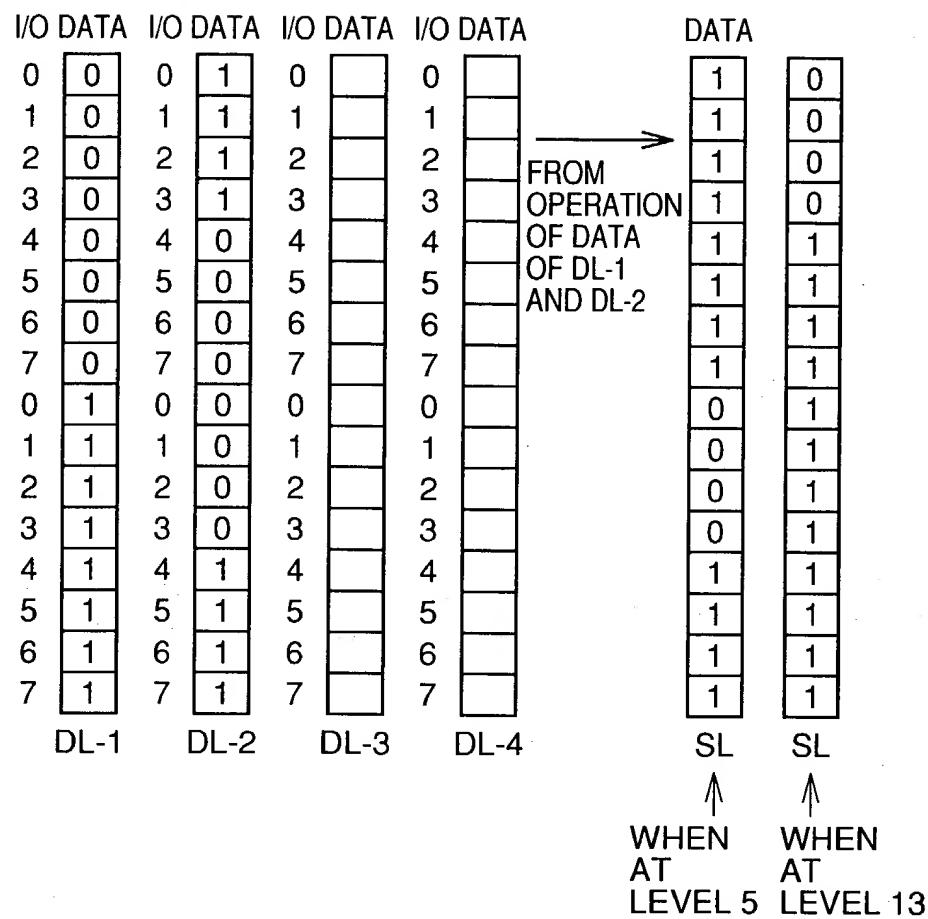




FIG.85

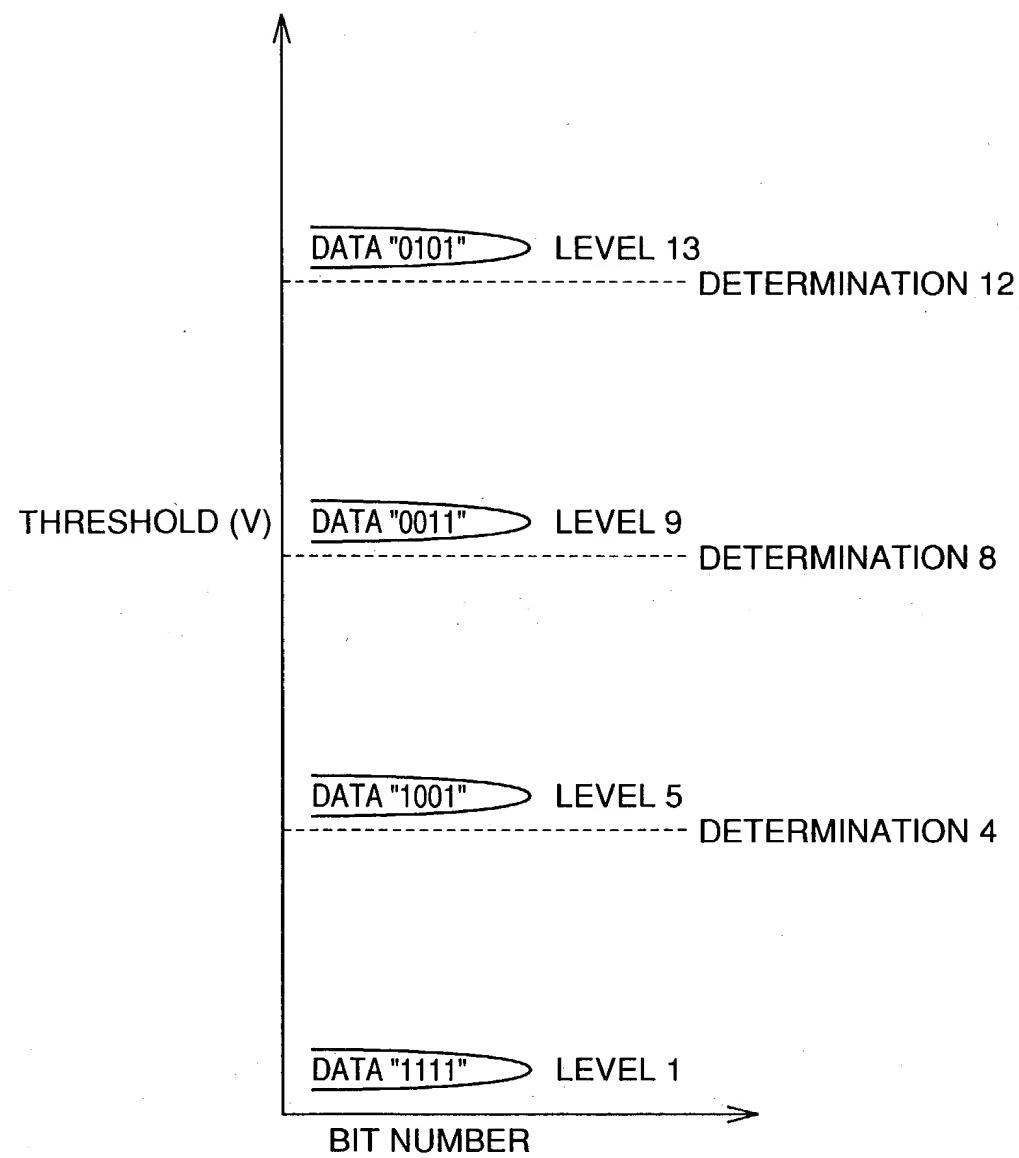




FIG.86

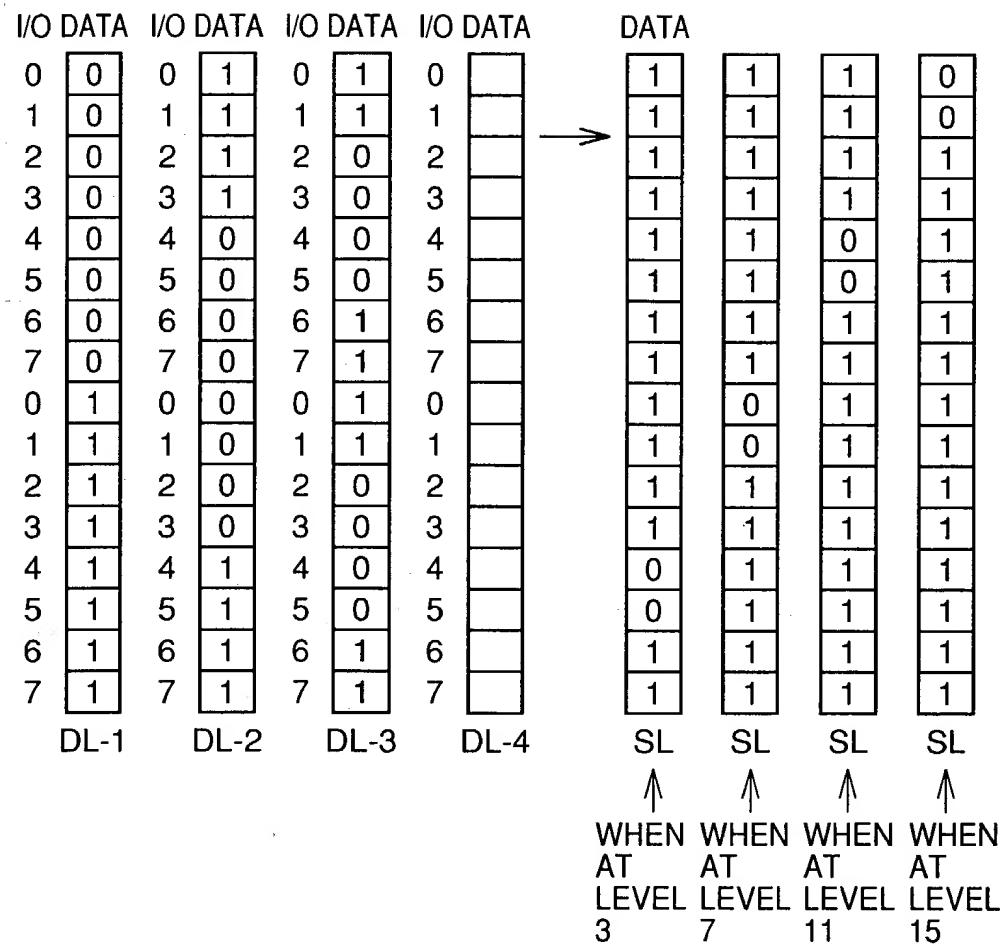




FIG.87

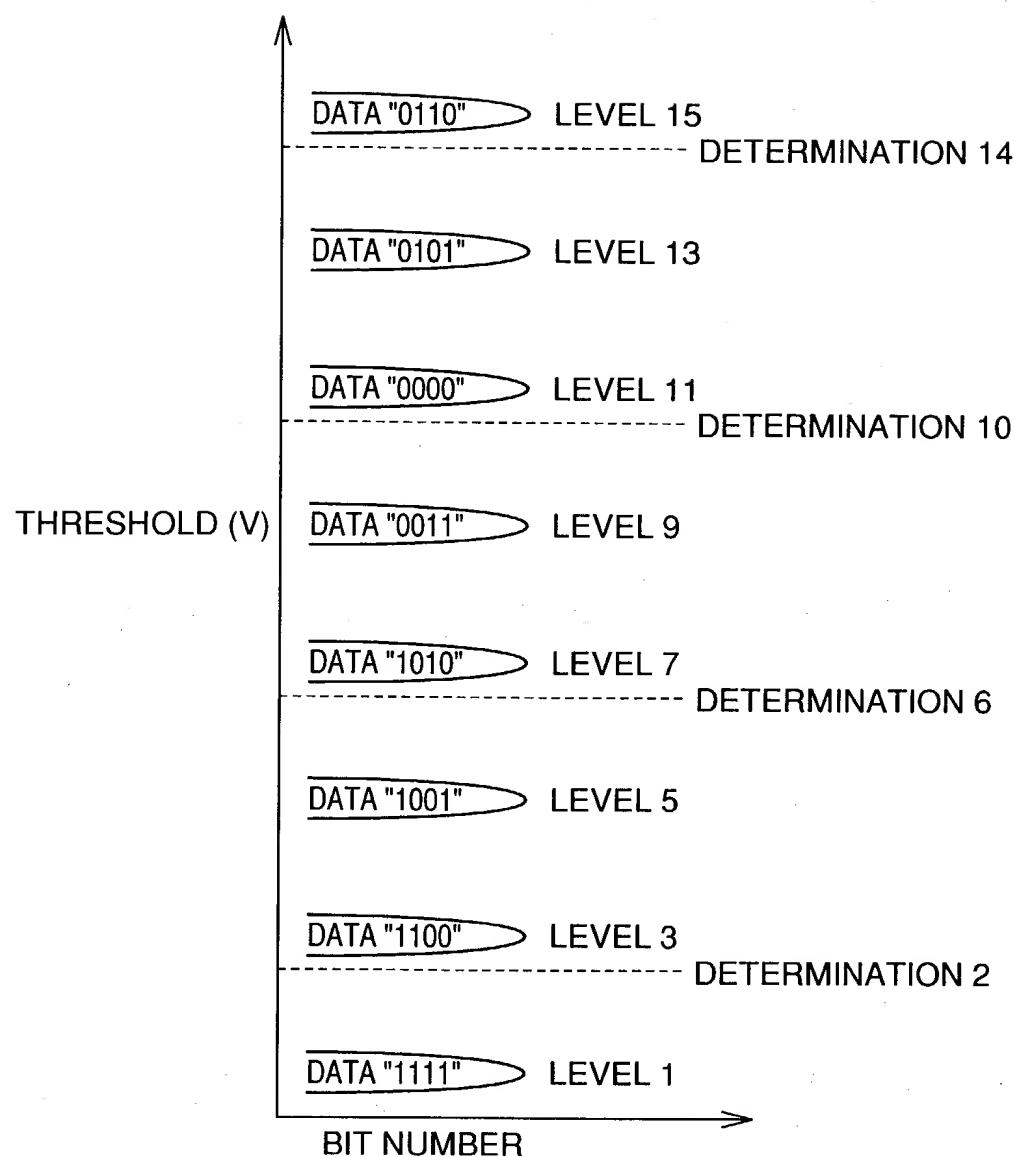




FIG.88

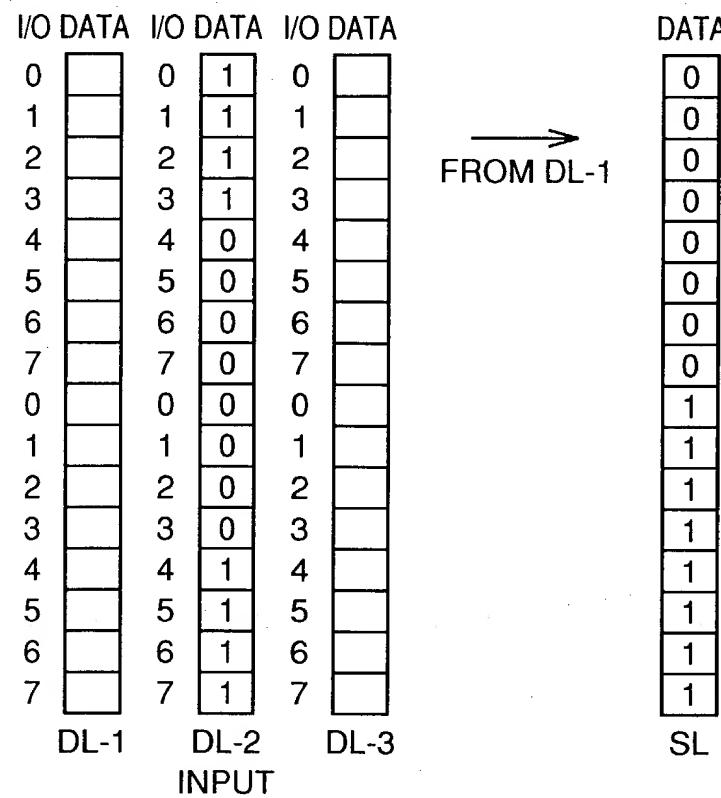




FIG.89

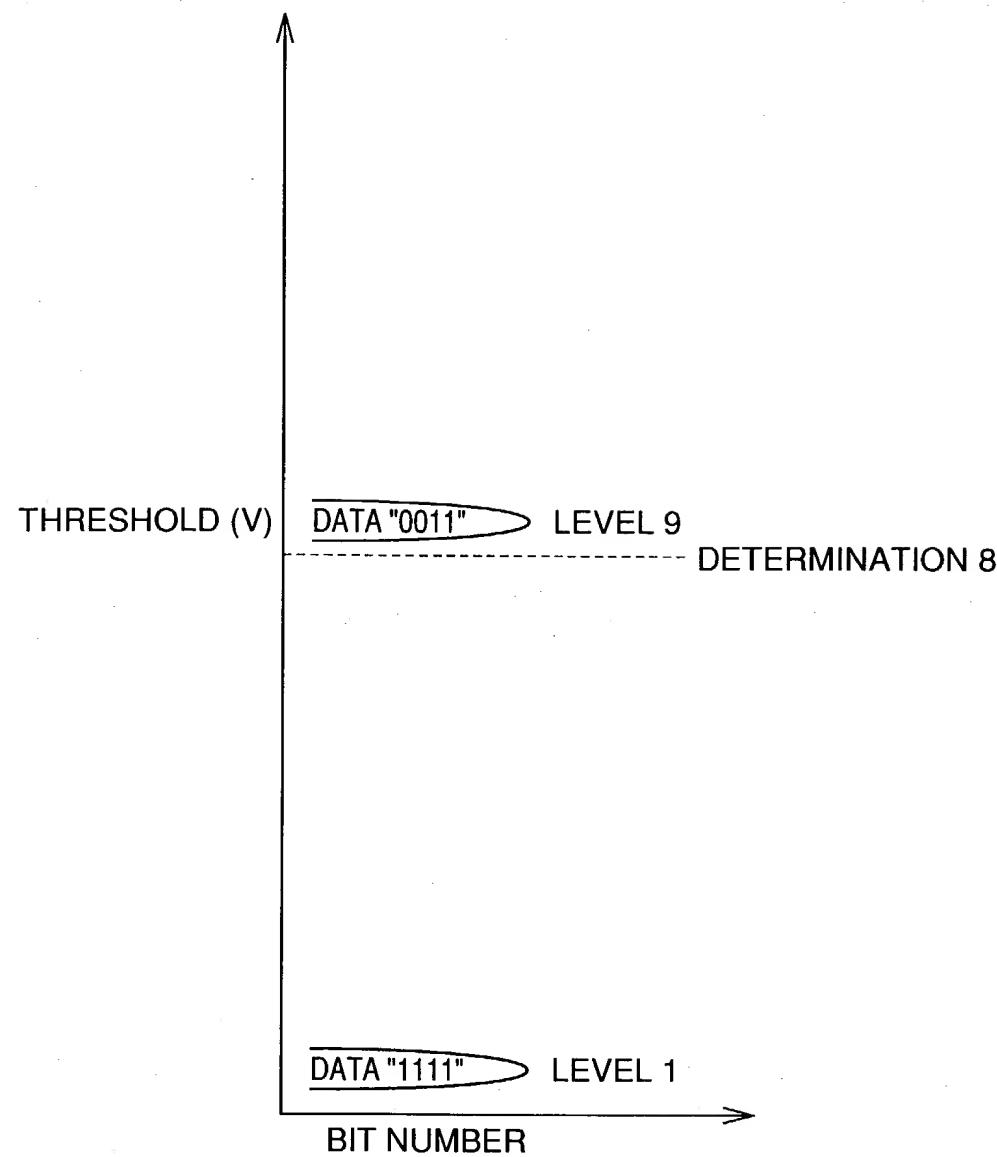




FIG.90

	I/O DATA	I/O DATA	I/O DATA		DATA
0		0 1	0 1		1 0
1		1 1	1 1		1 0
2		2 1	2 0	OPERATE DATA OF SL AND DL-2	1 0
3		3 1	3 0		1 1
4		4 0	4 0		1 1
5		5 0	5 0		1 1
6		6 0	6 1		1 1
7		7 0	7 1		1 1
0		0 0	0 1		0 1
1		1 0	1 1		0 1
2		2 0	2 0		0 1
3		3 0	3 0		0 1
4		4 1	4 0		1 1
5		5 1	5 0		1 1
6		6 1	6 1		1 1
7		7 1	7 1		1 1
	DL-1	DL-2	DL-3		SL LEVEL 13
			INPUT		LEVEL 5



FIG.91

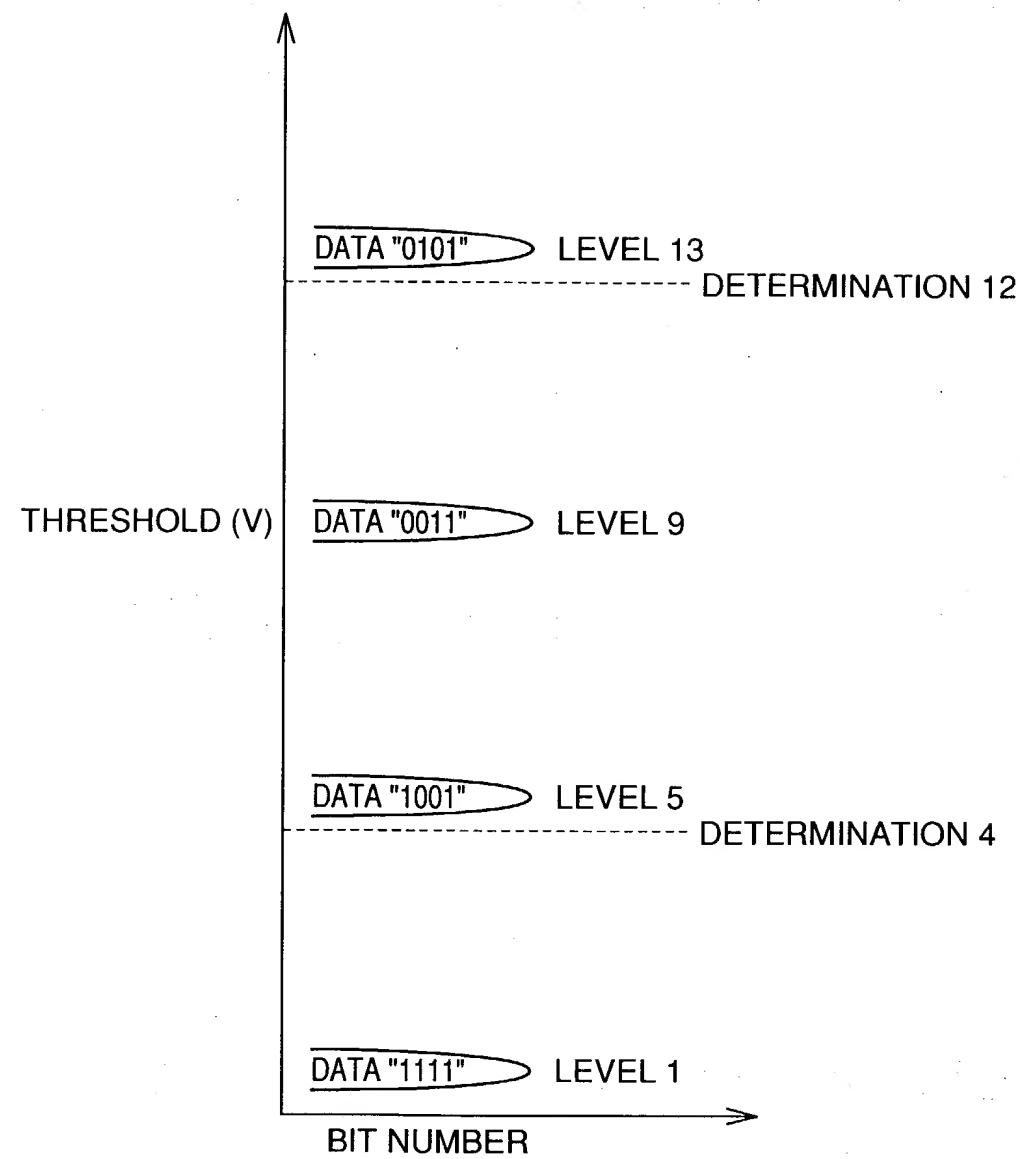




FIG. 92

I/O DATA		I/O DATA		I/O DATA		DATA	
0	1	0	1	0	1	0	0
1	1	1	0	1	1	0	0
2	1	2	0	2	0	0	0
3	1	3	1	3	0	0	0
4	1	4	1	4	0	0	0
5	1	5	0	5	0	0	0
6	1	6	0	6	1	0	0
7	1	7	1	7	1	0	0
0	0	0	1	0	1	1	1
1	0	1	0	1	1	1	1
2	0	2	0	2	0	1	1
3	0	3	1	3	0	1	1
4	0	4	1	4	0	1	1
5	0	5	0	5	0	1	1
6	0	6	0	6	1	1	1
7	0	7	1	7	1	1	1
DL-1		DL-2		DL-3		SL	
INPUT				READ AT DETERMINATION 8			



FIG.93

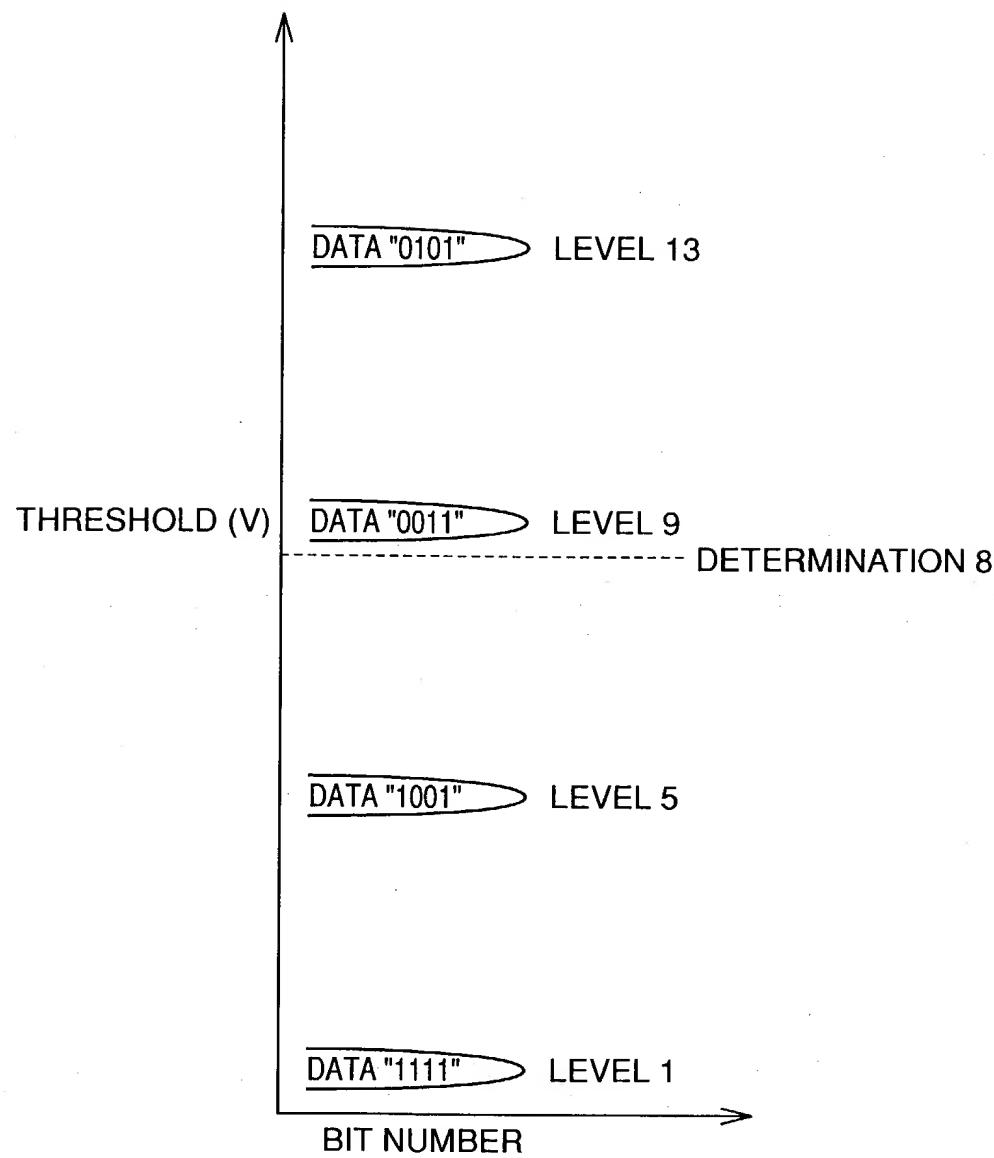




FIG.94

	I/O DATA	I/O DATA	I/O DATA		DATA
0	1	0	1	0	0
1	1	1	0	1	0
2	1	2	0	2	0
3	1	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	1
7	1	7	1	7	1
0	0	0	1	0	0
1	0	1	0	1	0
2	0	2	0	2	0
3	0	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	1
7	1	7	1	7	1

DL-1 DL-2 DL-3 SL

INPUT READ AT DETERMINATION 4

OR DATA OF SL AND DL-1 AND STORE RESULT IN DL-1



FIG.95

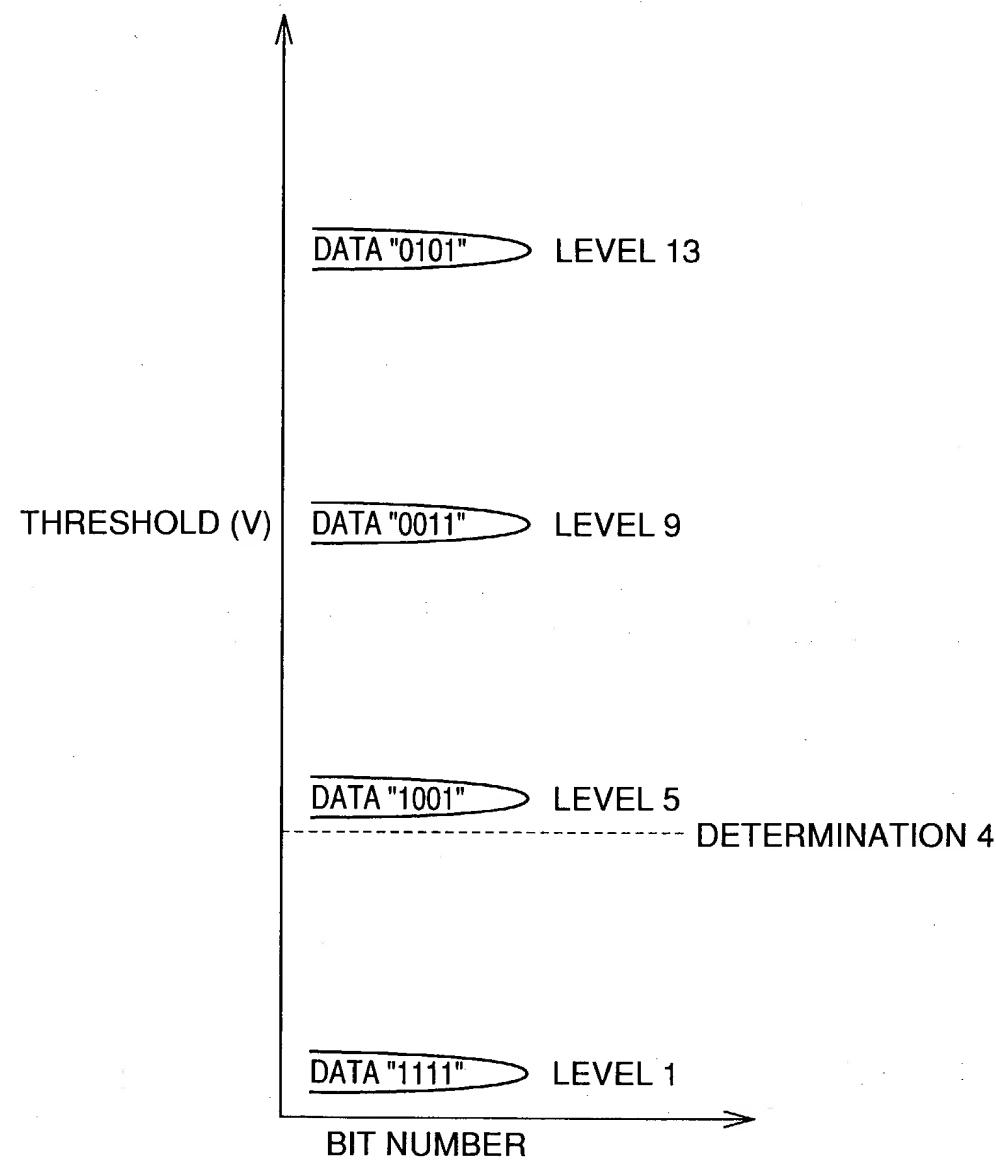
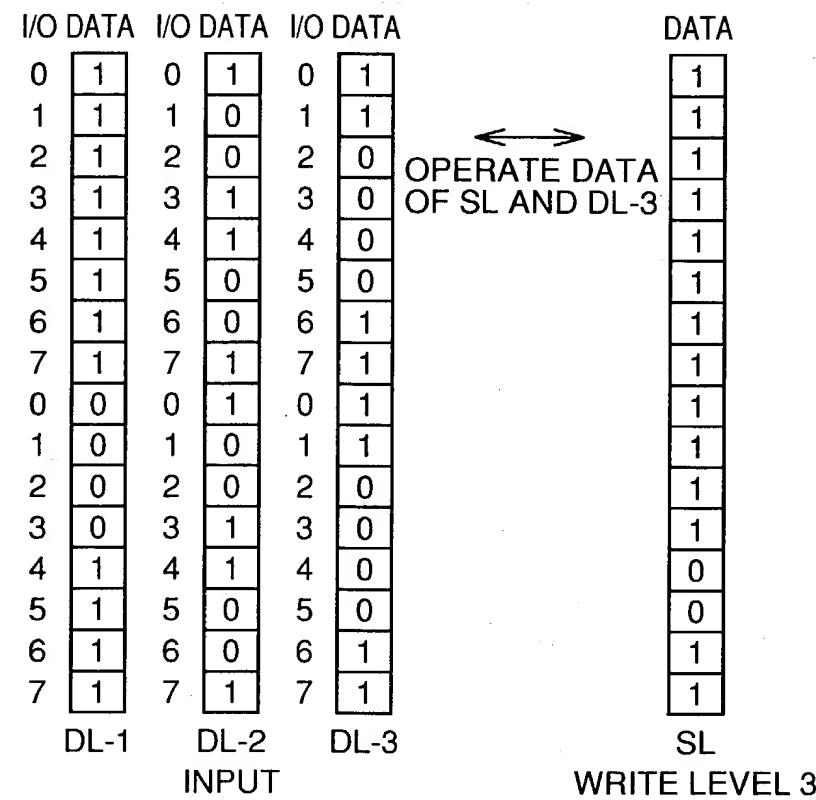




FIG. 96



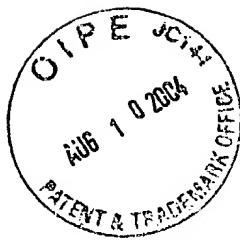


FIG.97

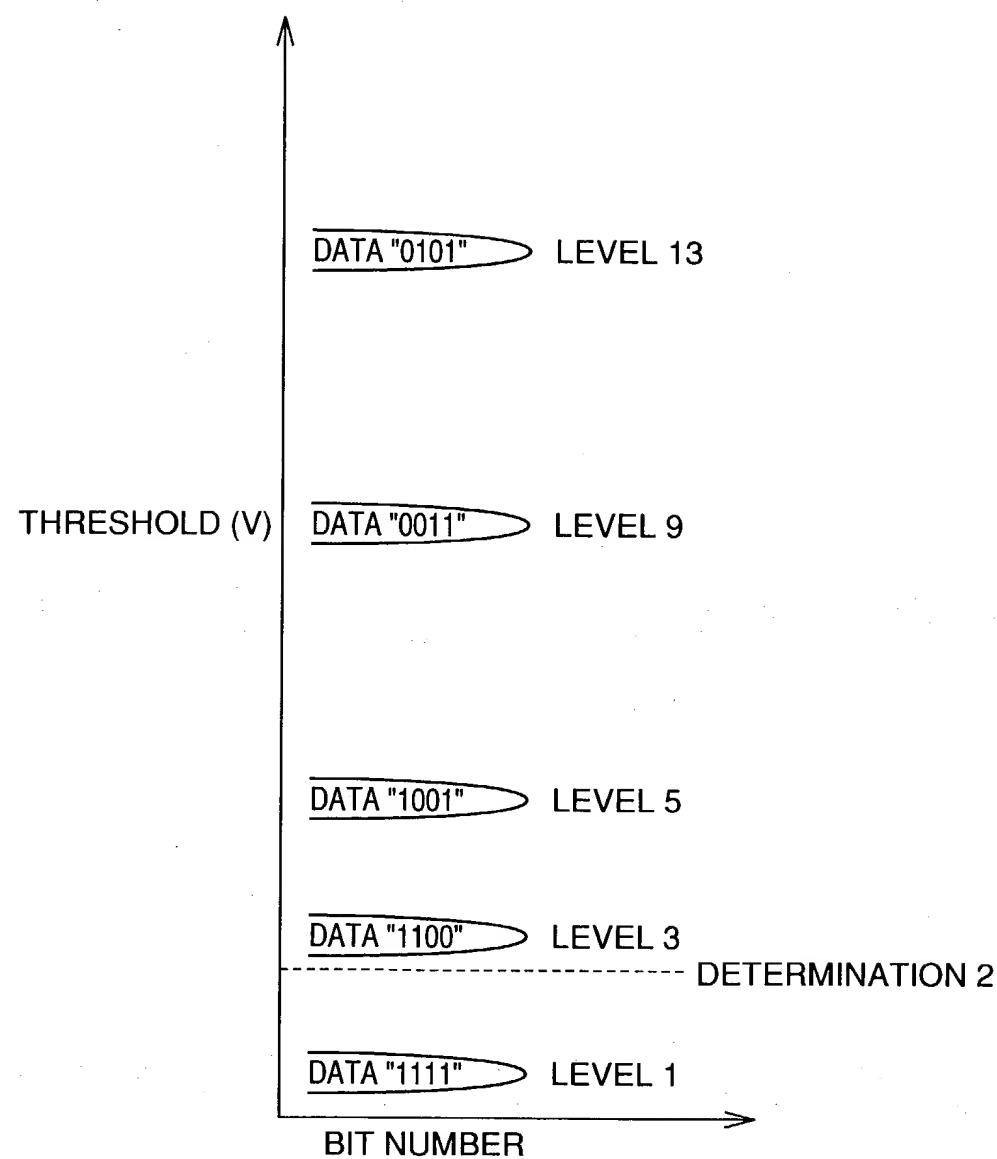




FIG.98

	I/O DATA	I/O DATA	I/O DATA		DATA
0	1	0	1	0	1
1	1	1	0	1	1
2	1	2	0	2	0
3	1	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	1
7	1	7	1	7	1
0	0	0	1	0	0
1	0	1	0	1	0
2	0	2	0	2	0
3	0	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	1
7	1	7	1	7	1

DL-1 DL-2 DL-3 INPUT OPERATE DATA OF DL-1 AND DL-3 TO SL DATA

SL WRITE LEVEL 7

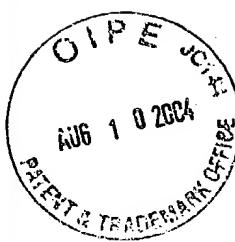


FIG. 99

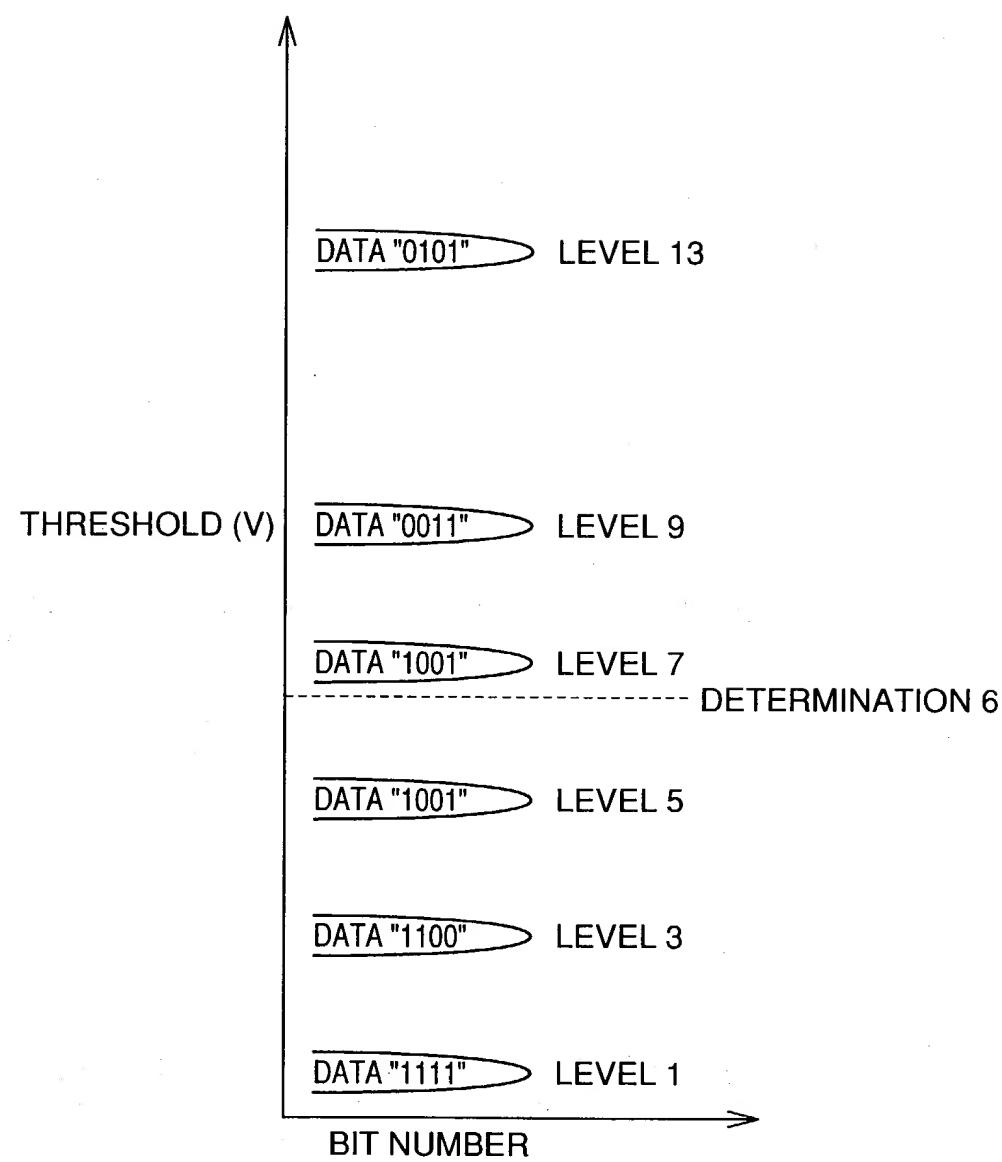




FIG. 100

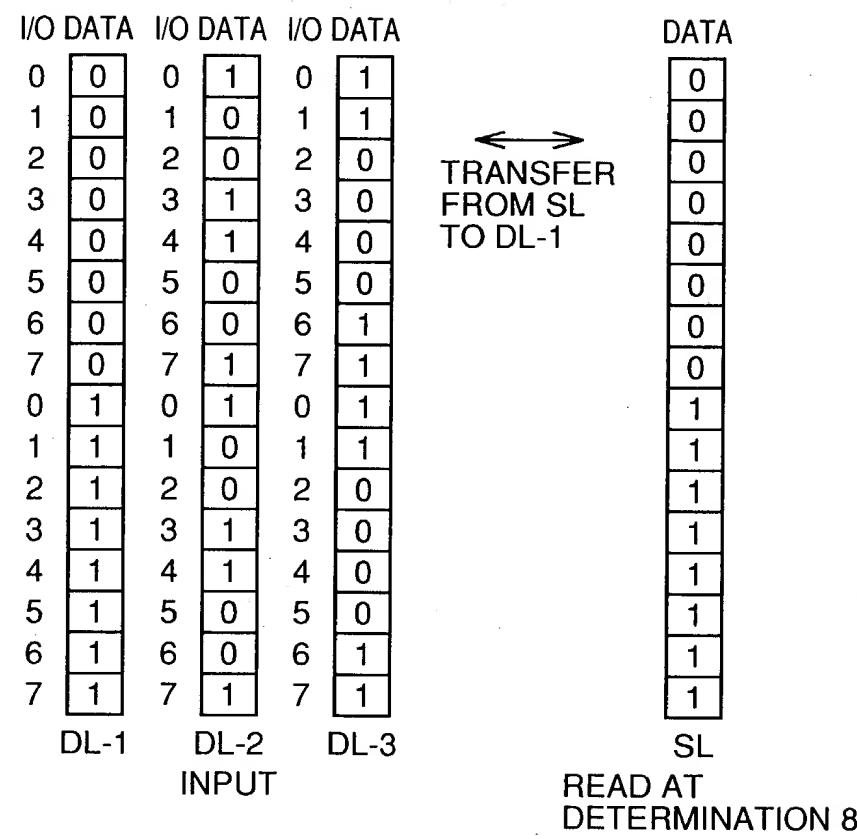




FIG. 101

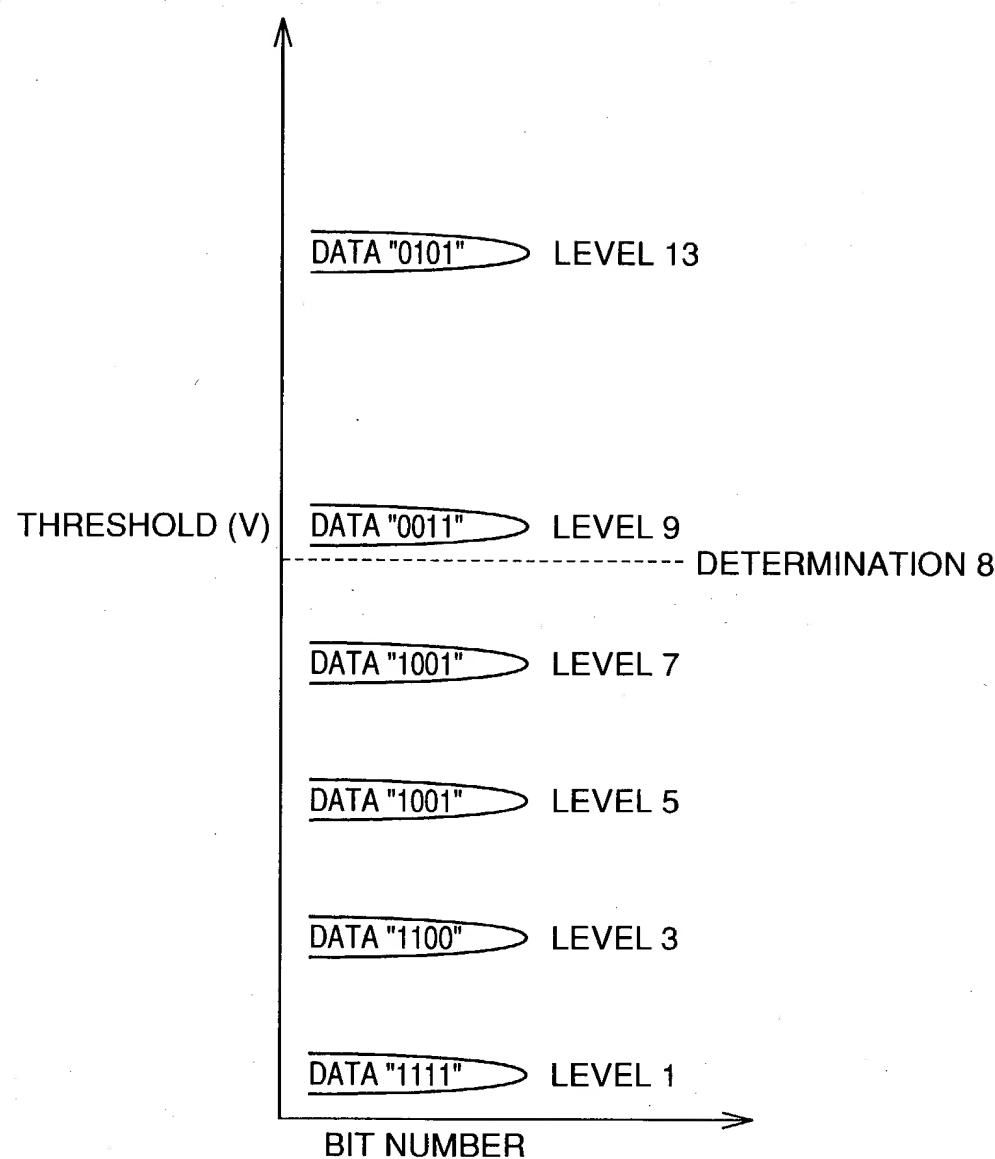




FIG. 102

	I/O DATA	I/O DATA	I/O DATA		DATA
0	1	0	1	0	1
1	1	1	0	1	1
2	1	2	0	2	0
3	1	3	1	3	0
4	0	4	1	4	0
5	0	5	0	5	0
6	0	6	0	6	1
7	0	7	1	7	1
0	1	0	1	0	1
1	1	1	0	1	1
2	1	2	0	2	0
3	1	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	1
7	1	7	1	7	1

DL-1 DL-2 DL-3 INPUT

OR INVERTED DATA OF SL AND DATA OF DL-1 AND STORE RESULT IN DL-1

SL

READ AT DETERMINATION 12



FIG. 103

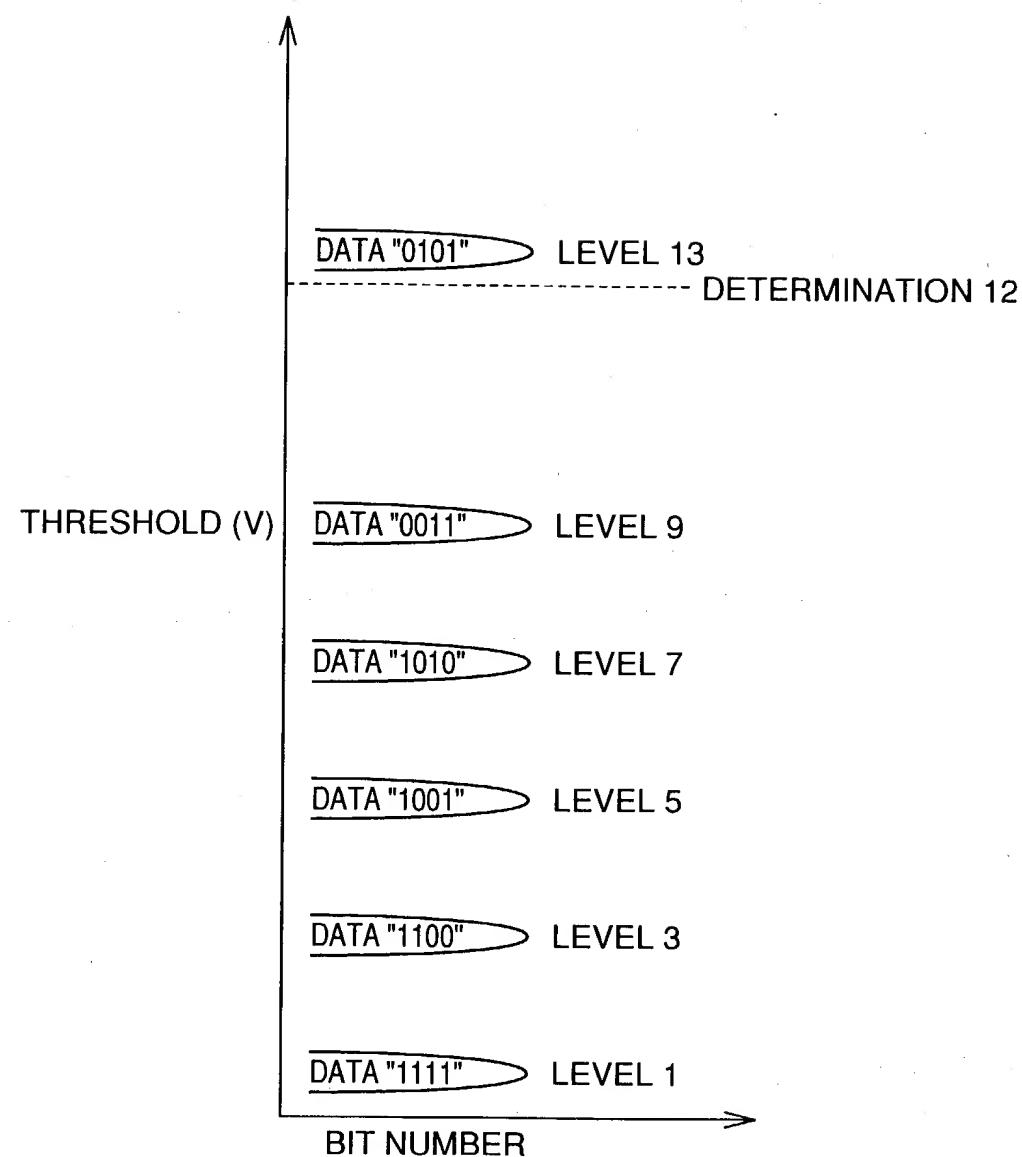




FIG. 104

	I/O DATA	I/O DATA	I/O DATA		DATA
0	1	0	1	0	1
1	1	1	0	1	1
2	1	2	0	2	0
3	1	3	1	3	1
4	0	4	1	4	0
5	0	5	0	5	0
6	0	6	0	6	1
7	0	7	1	7	1
0	1	0	1	0	1
1	1	1	0	1	1
2	1	2	0	2	0
3	1	3	1	3	1
4	1	4	1	4	1
5	1	5	0	5	1
6	1	6	0	6	1
7	1	7	1	7	1

DL-1 DL-2 DL-3 INPUT OPERATE DATA
OF DL-1 AND
DL-3
TO SL

DATA

SL

WRITE LEVEL 11



FIG. 105

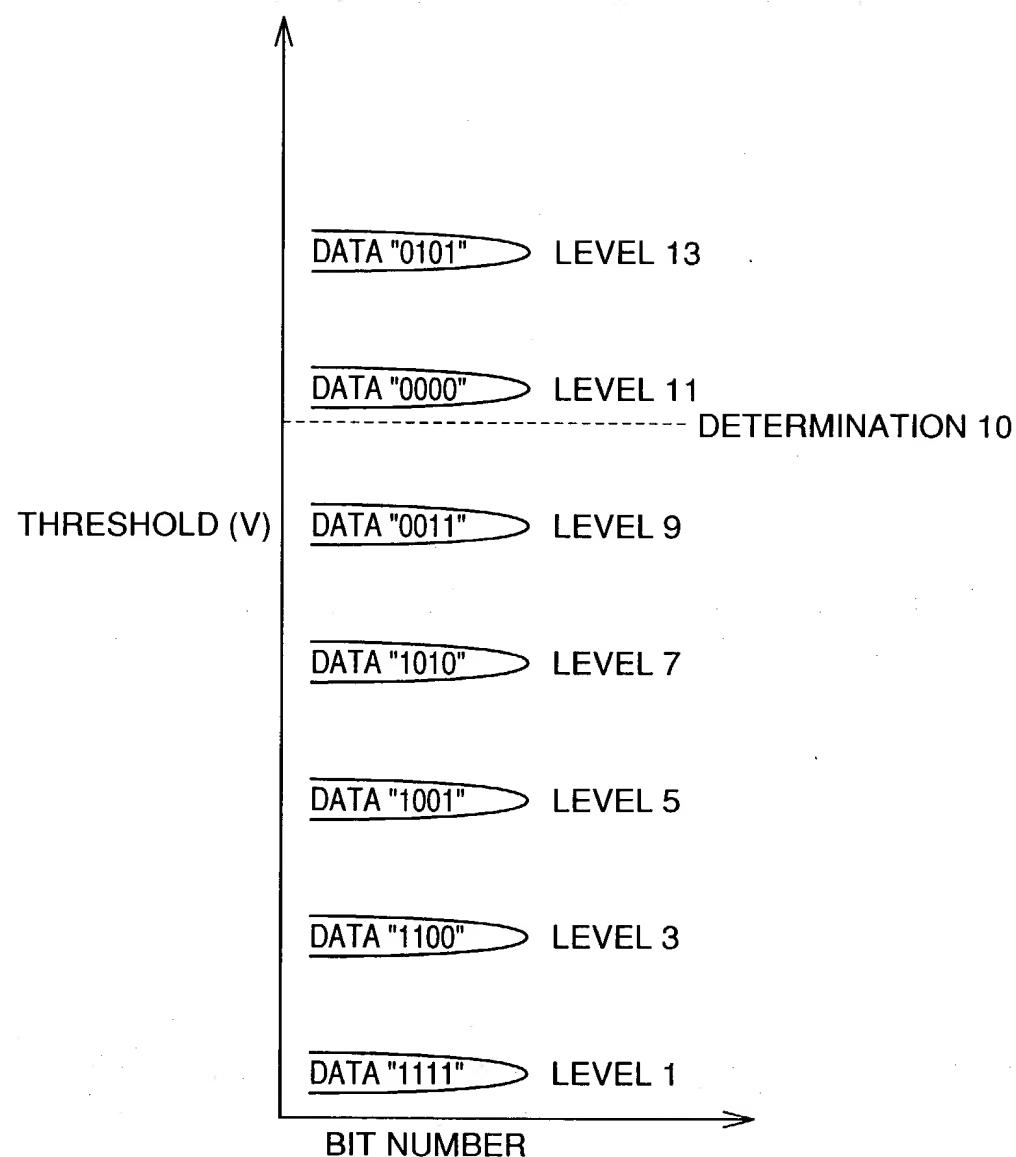




FIG. 106

	I/O DATA	I/O DATA	I/O DATA		DATA
0	1	0	1	0	0
1	1	1	0	1	0
2	1	2	0	2	0
3	1	3	1	3	0
4	0	4	1	4	0
5	0	5	0	5	0
6	0	6	0	6	1
7	0	7	1	7	1
0	0	0	1	0	1
1	0	1	0	1	1
2	0	2	0	2	0
3	0	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	1
7	1	7	1	7	1

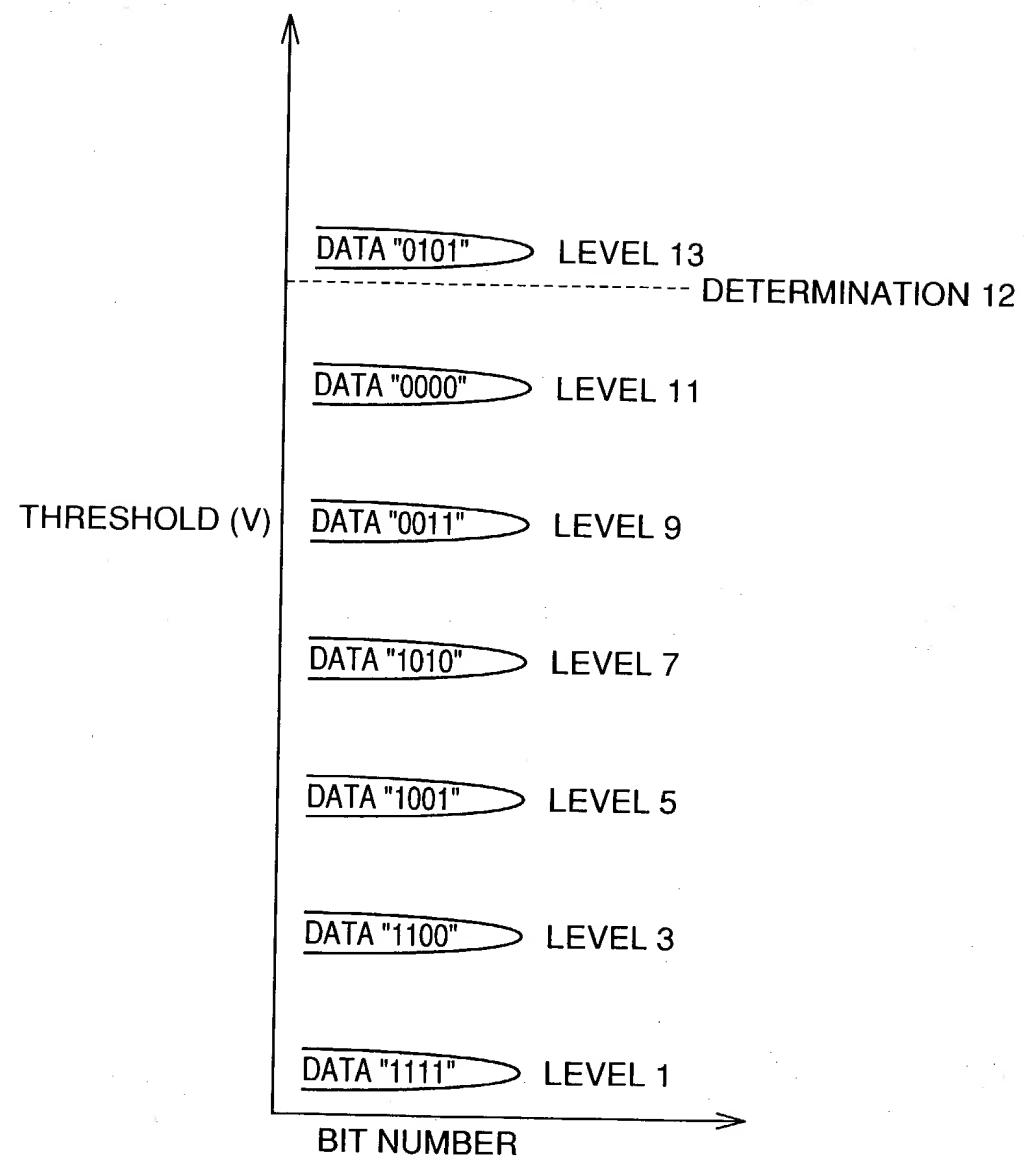
DL-1 DL-2 DL-3 INPUT SL DATA

OPERATE DATA
OF DL-1 AND
DL-3
TO SL

READ AT
DETERMINATION 12



FIG. 107



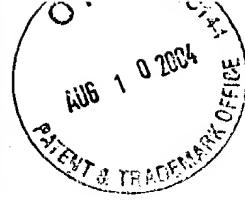


FIG. 108

I/O DATA	I/O DATA	I/O DATA	DATA
0	0	0	0
1	1	1	0
2	2	2	1
3	3	3	1
4	4	4	1
5	5	5	1
6	6	6	1
7	7	7	1
0	0	0	1
1	1	1	1
2	2	2	1
3	3	3	1
4	4	4	1
5	5	5	1
6	6	6	1
7	7	7	1

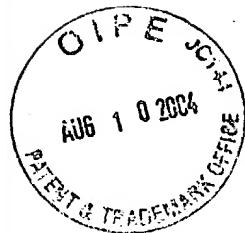


FIG. 109

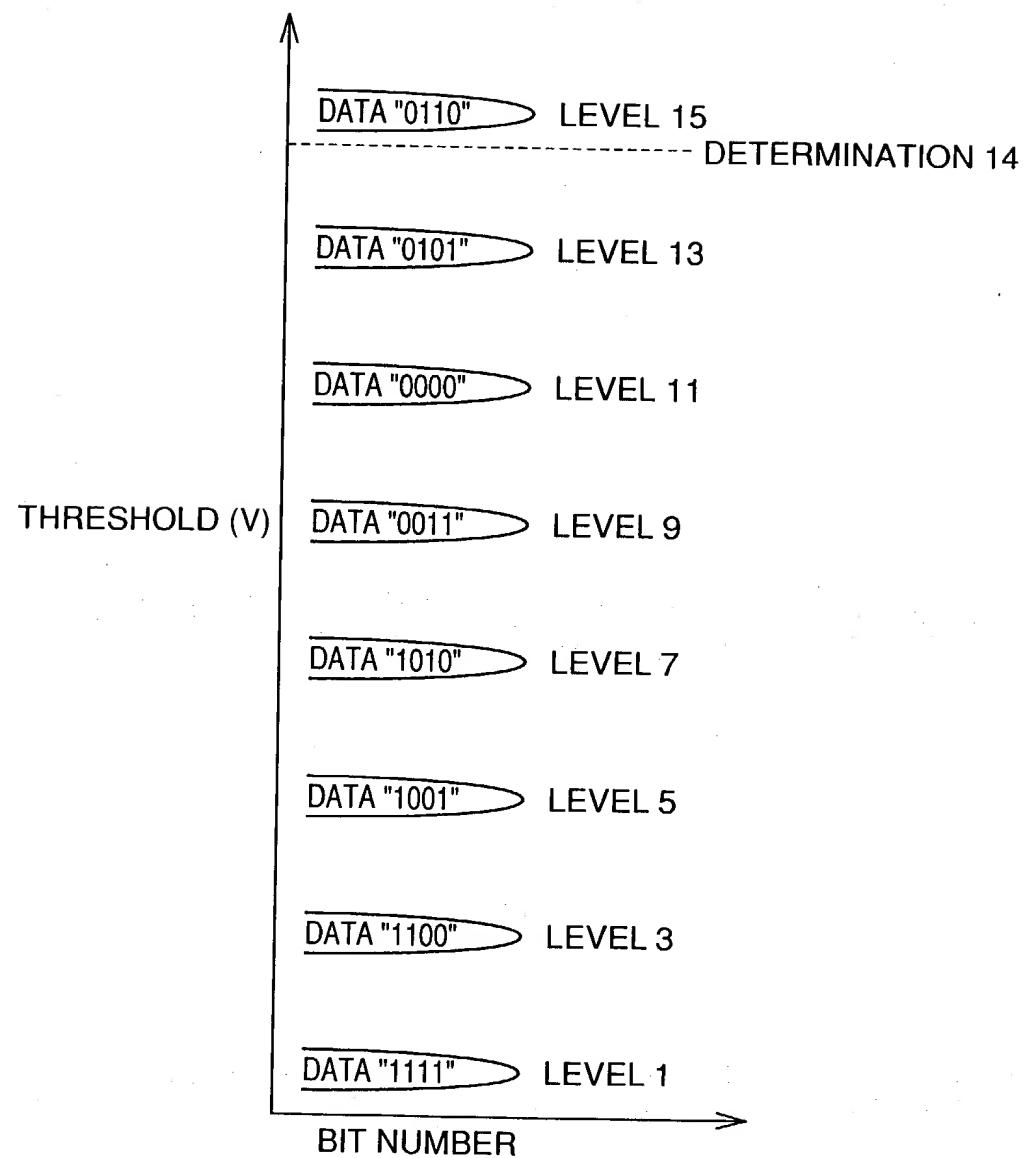




FIG. 110

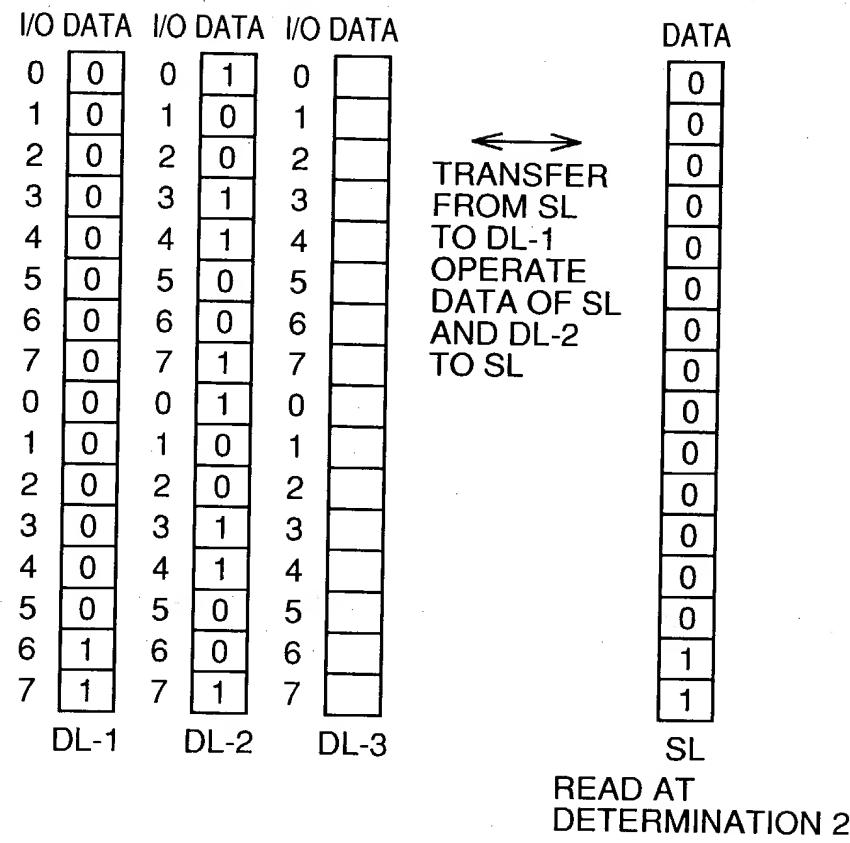




FIG. 111

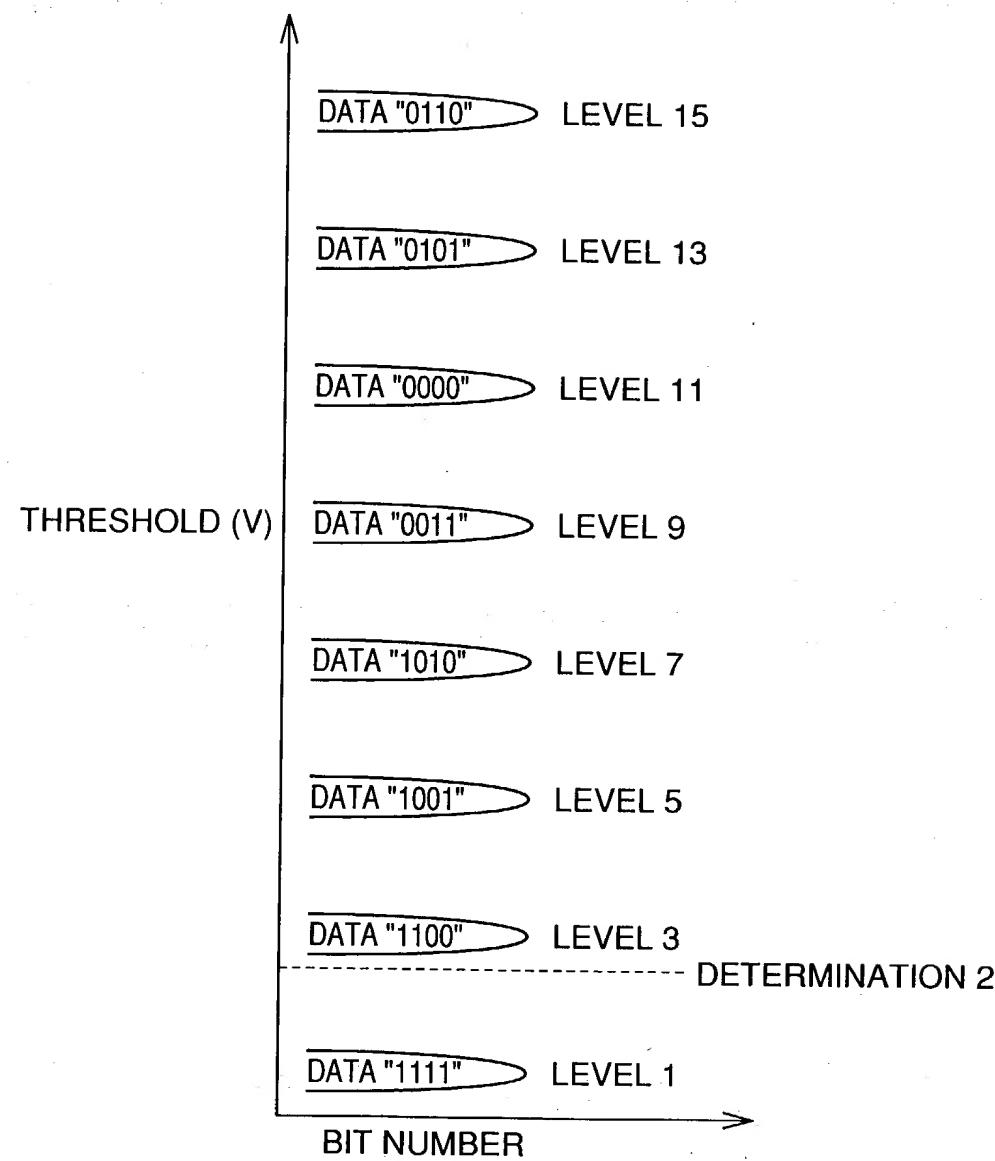




FIG. 112

	I/O DATA	I/O DATA	I/O DATA	DATA
0	0	0	1	0
1	0	1	0	1
2	0	2	0	2
3	0	3	1	3
4	0	4	1	4
5	0	5	0	5
6	0	6	0	6
7	0	7	1	7
0	0	0	1	0
1	0	1	0	1
2	0	2	0	2
3	0	3	1	3
4	0	4	1	4
5	0	5	0	5
6	1	6	0	6
7	1	7	1	7

DL-1 DL-2 DL-3 SL

WRITE LEVEL 2



FIG. 113

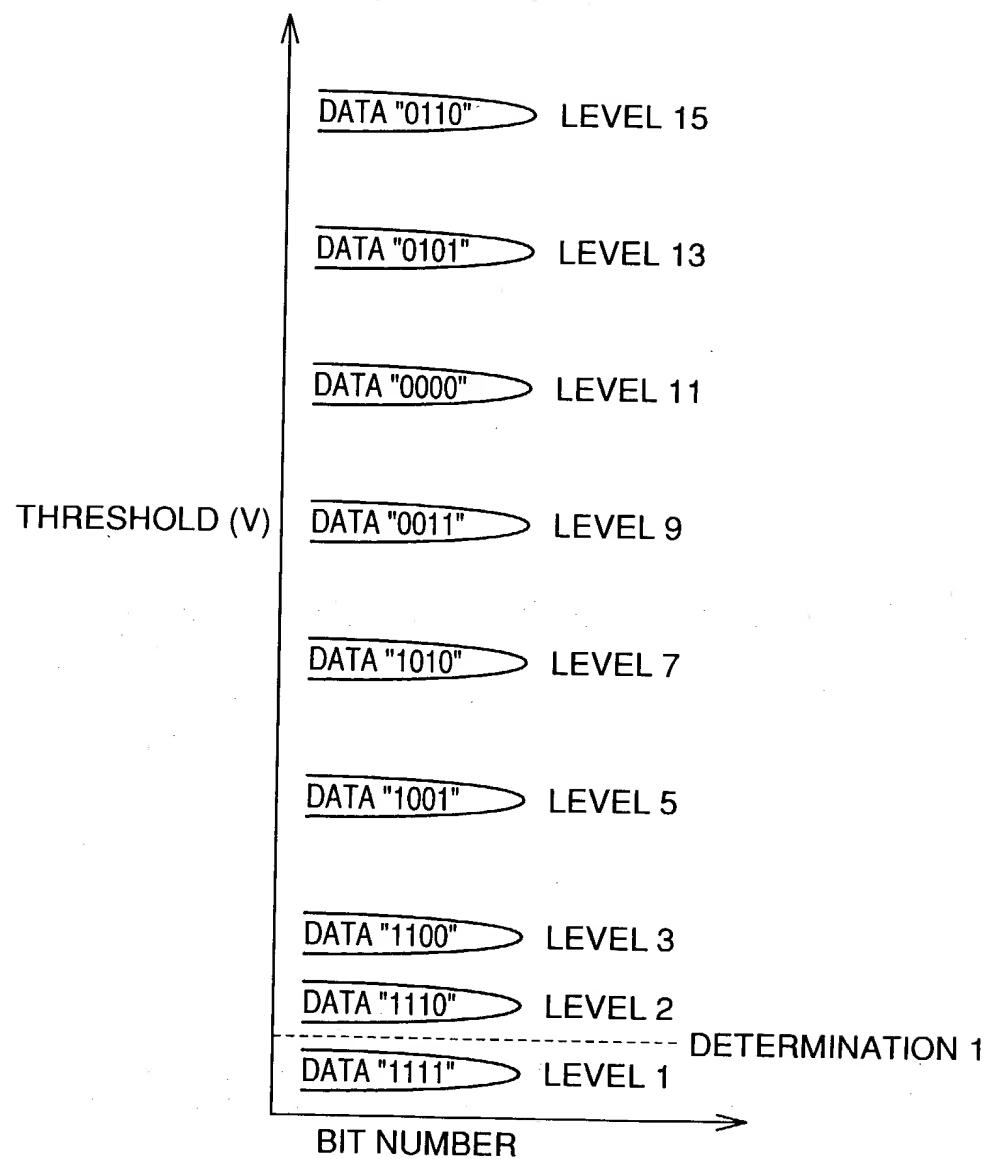




FIG. 114

	I/O DATA	I/O DATA	I/O DATA		DATA
0	1	0	1	0	0
1	1	1	0	1	0
2	1	2	0	2	0
3	1	3	1	3	0
4	1	4	1	4	0
5	1	5	0	5	0
6	1	6	0	6	0
7	1	7	1	7	0
0	1	0	1	0	0
1	1	1	0	1	0
2	1	2	0	2	0
3	1	3	1	3	0
4	0	4	1	4	1
5	0	5	0	5	1
6	1	6	0	6	1
7	1	7	1	7	1

OR INVERTED
DATA OF SL
AND DATA OF
DL-1 AND
STORE RESULT
IN DL-1

READ AT
DETERMINATION 4



FIG. 115

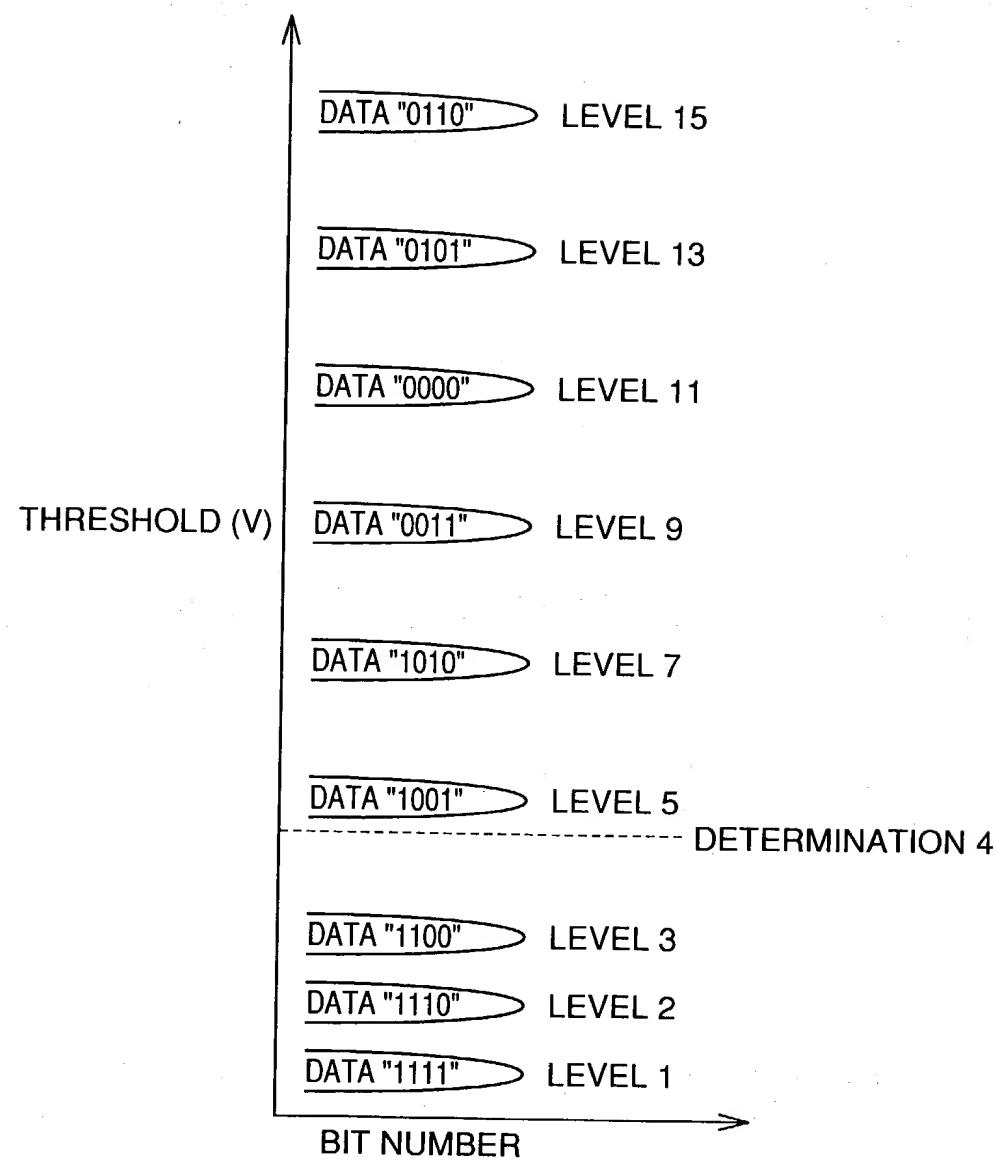




FIG. 116

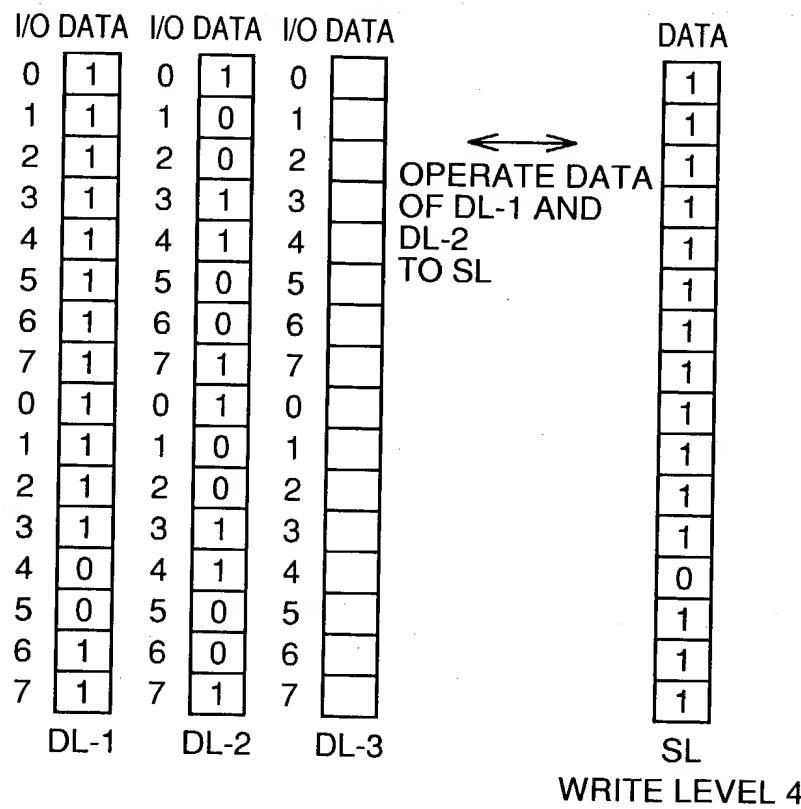




FIG. 117

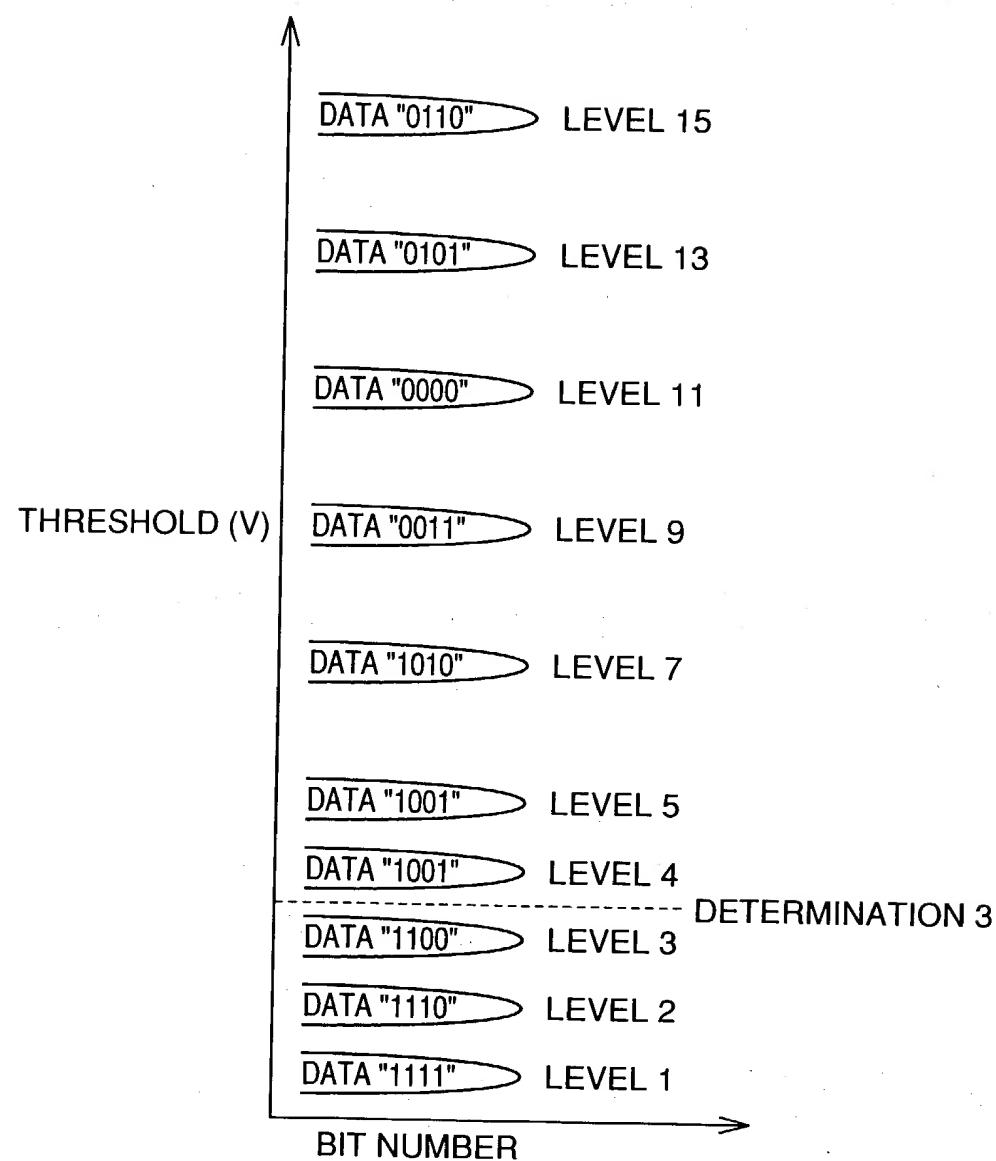
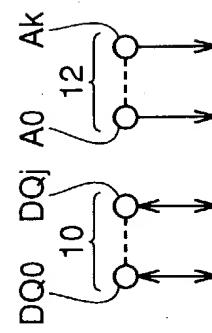




FIG. 118
PRIOR ART

8000



ADDRESS BUFFER/DATA INPUT/OUTPUT BUFFER

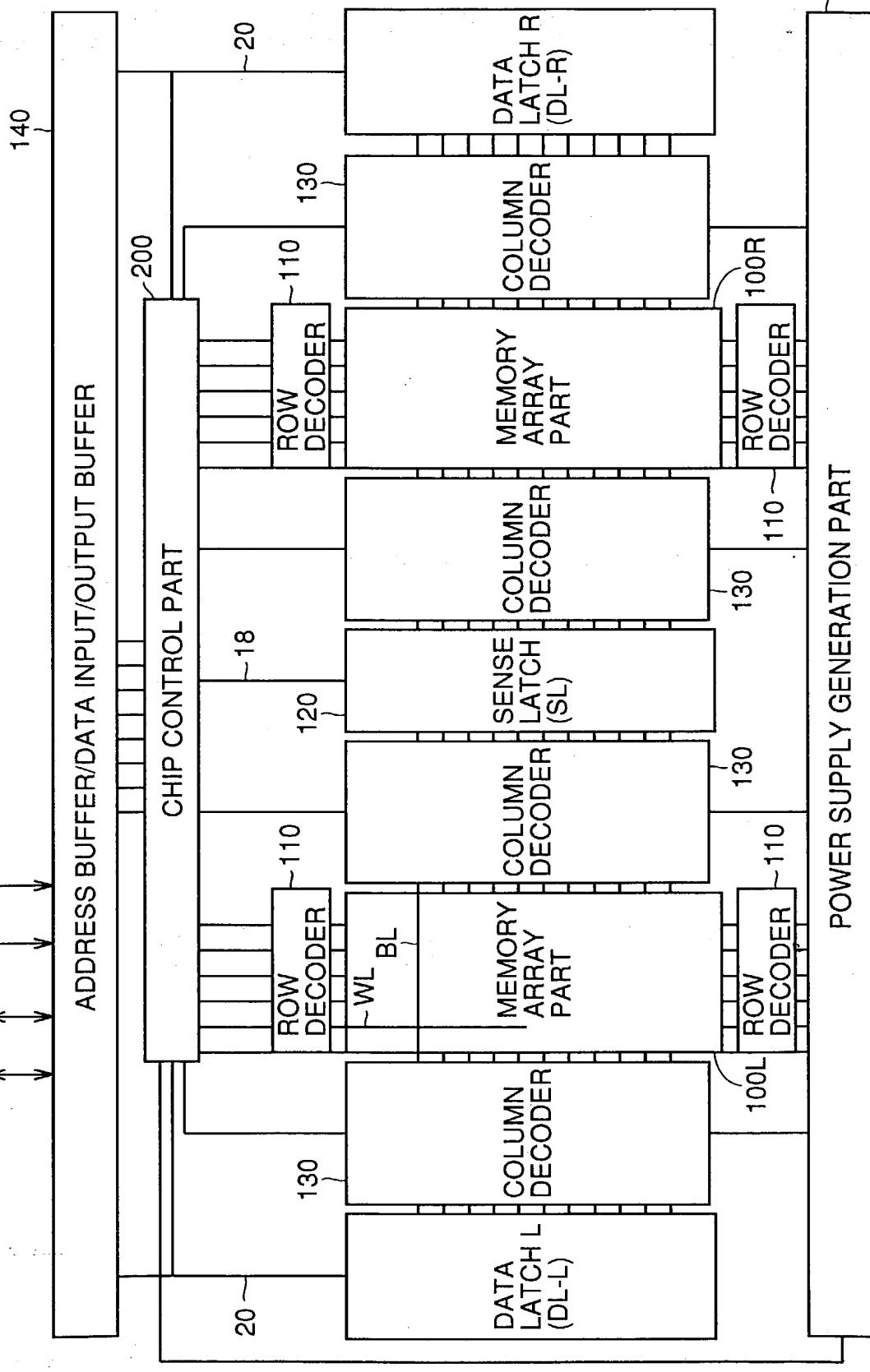




FIG. 119 PRIOR ART

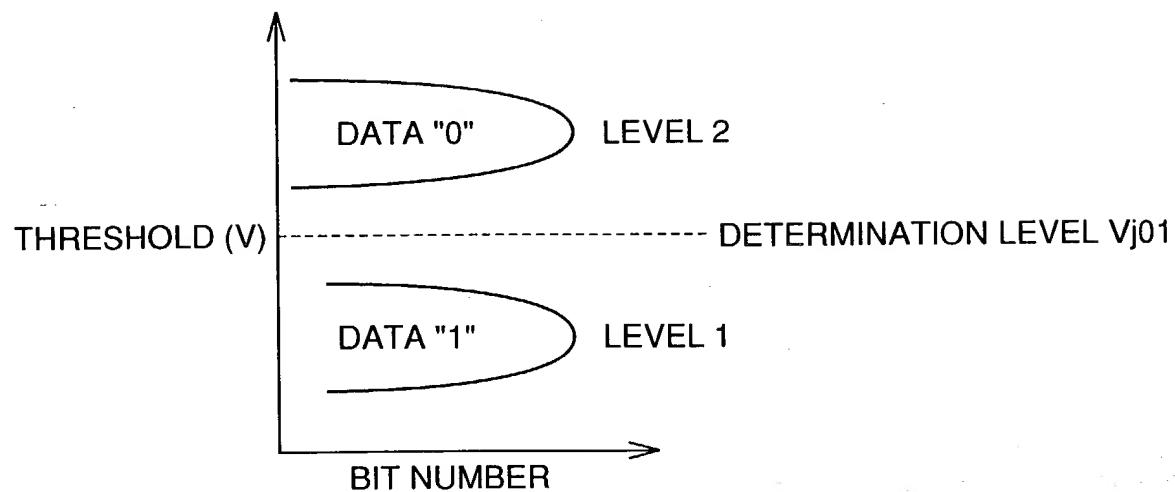


FIG. 120 PRIOR ART

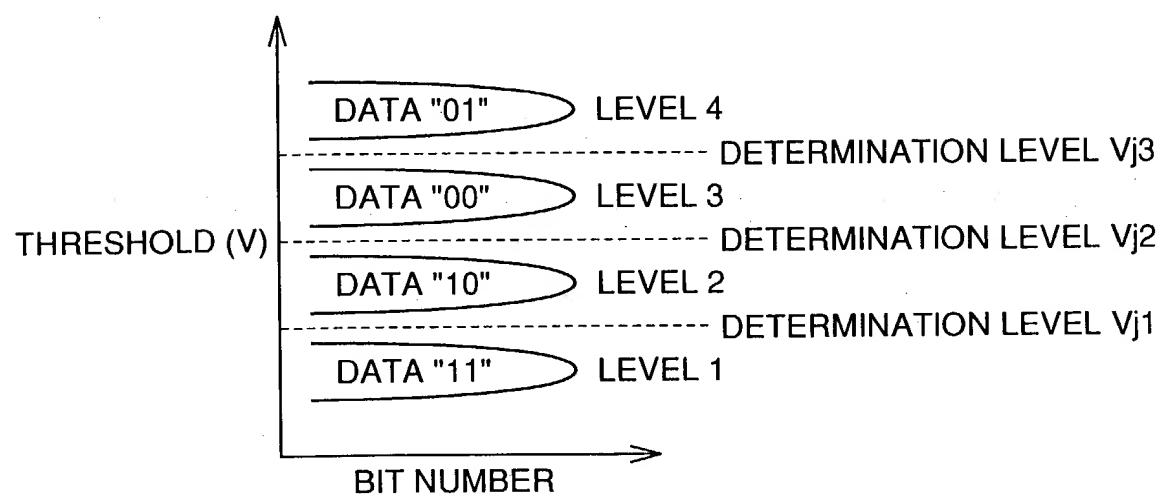




FIG. 121 PRIOR ART

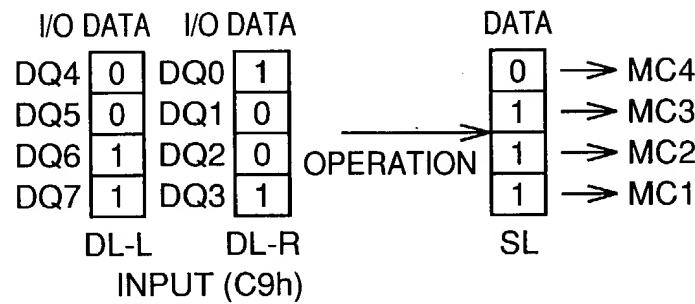


FIG. 122 PRIOR ART

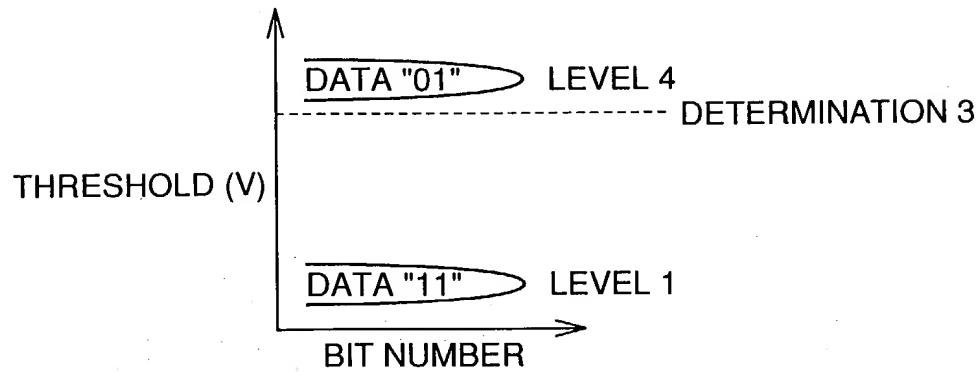




FIG. 123 PRIOR ART

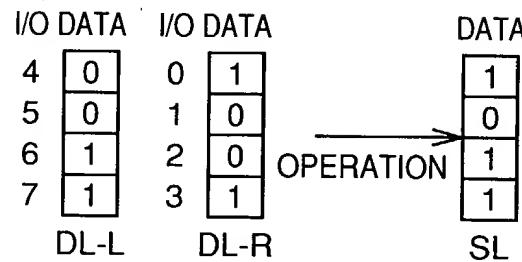


FIG. 124 PRIOR ART

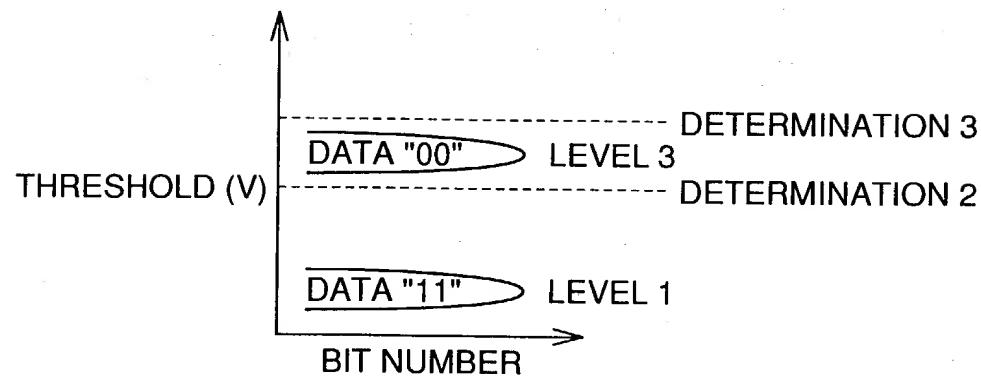




FIG. 125 PRIOR ART

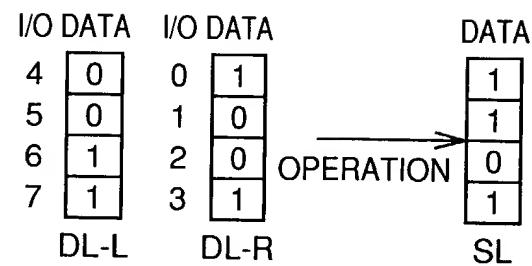


FIG. 126 PRIOR ART

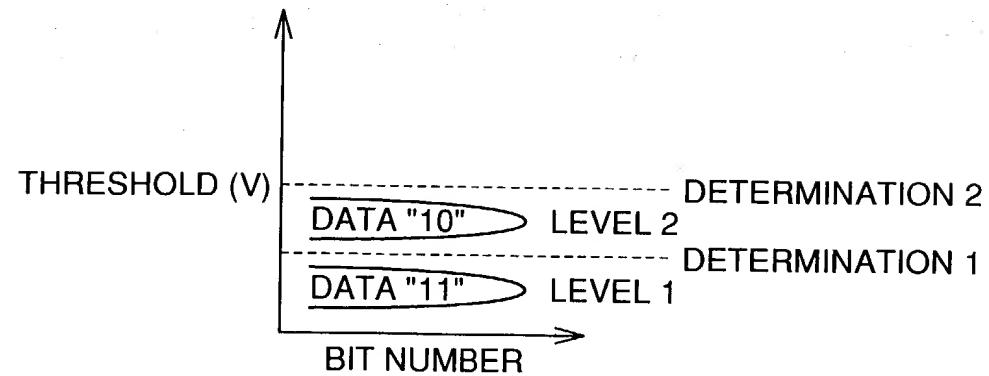




FIG. 127 PRIOR ART



FIG. 128 PRIOR ART

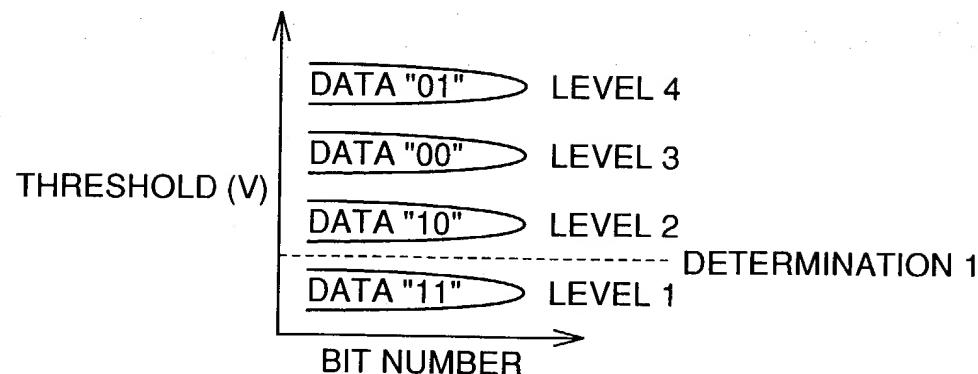




FIG. 129 PRIOR ART

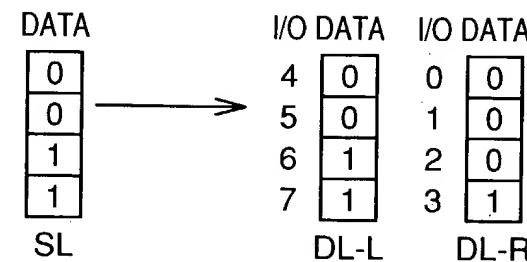


FIG. 130 PRIOR ART

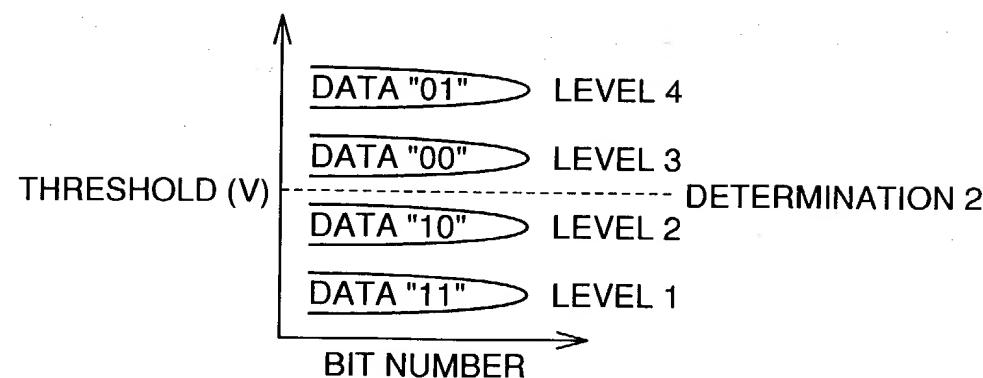




FIG. 131 PRIOR ART

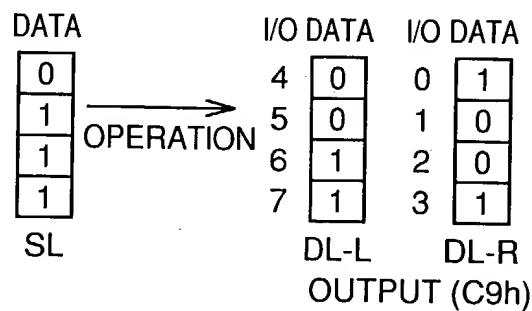


FIG. 132 PRIOR ART

